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OCT 30
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A champion of analog innovation Pg 22
Physics and economics Pg 10
Compact fluorescent lights: not always the best solution Pg 28
Design Ideas Pg 61
Tales from the Cube: Stick to the schematic Pg 70

CHOOSING THE RIGHT PROCESSOR CANDIDATE

MICROPROCESSOR DIRECTORY

Page 38

MULTICORE: THE FUTURE OF SOCs

Page 31

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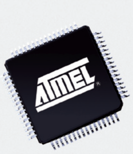

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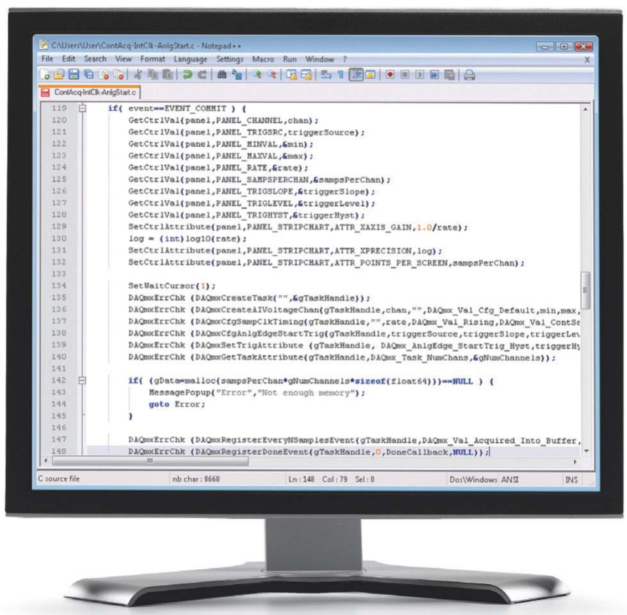

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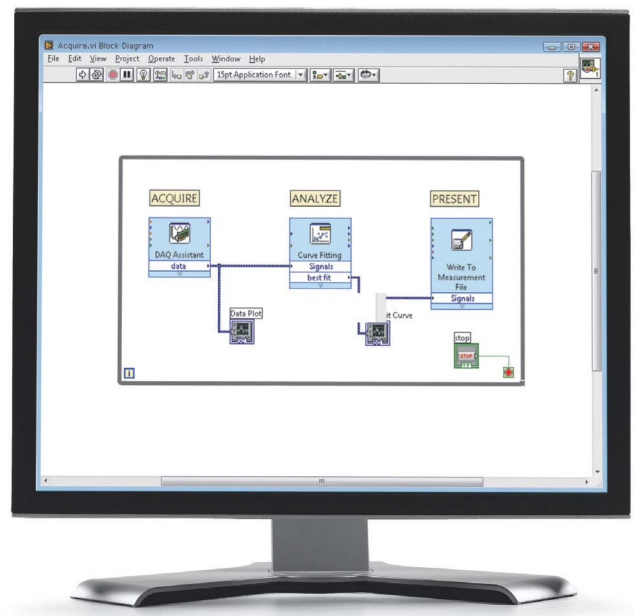

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EDN contents

10.30.08

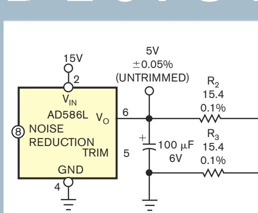
Multicore: the future of SOCs

31 Will systems on chips follow server CPUs down the road to having many identical processor cores on a die? *by Ron Wilson, Executive Editor*

Choosing the right processor candidate: the 35th annual microprocessor directory

38 Find the perfect processor candidates and development tools for your project. *by Robert Cravotta, Technical Editor*

DESIGNIDEAS

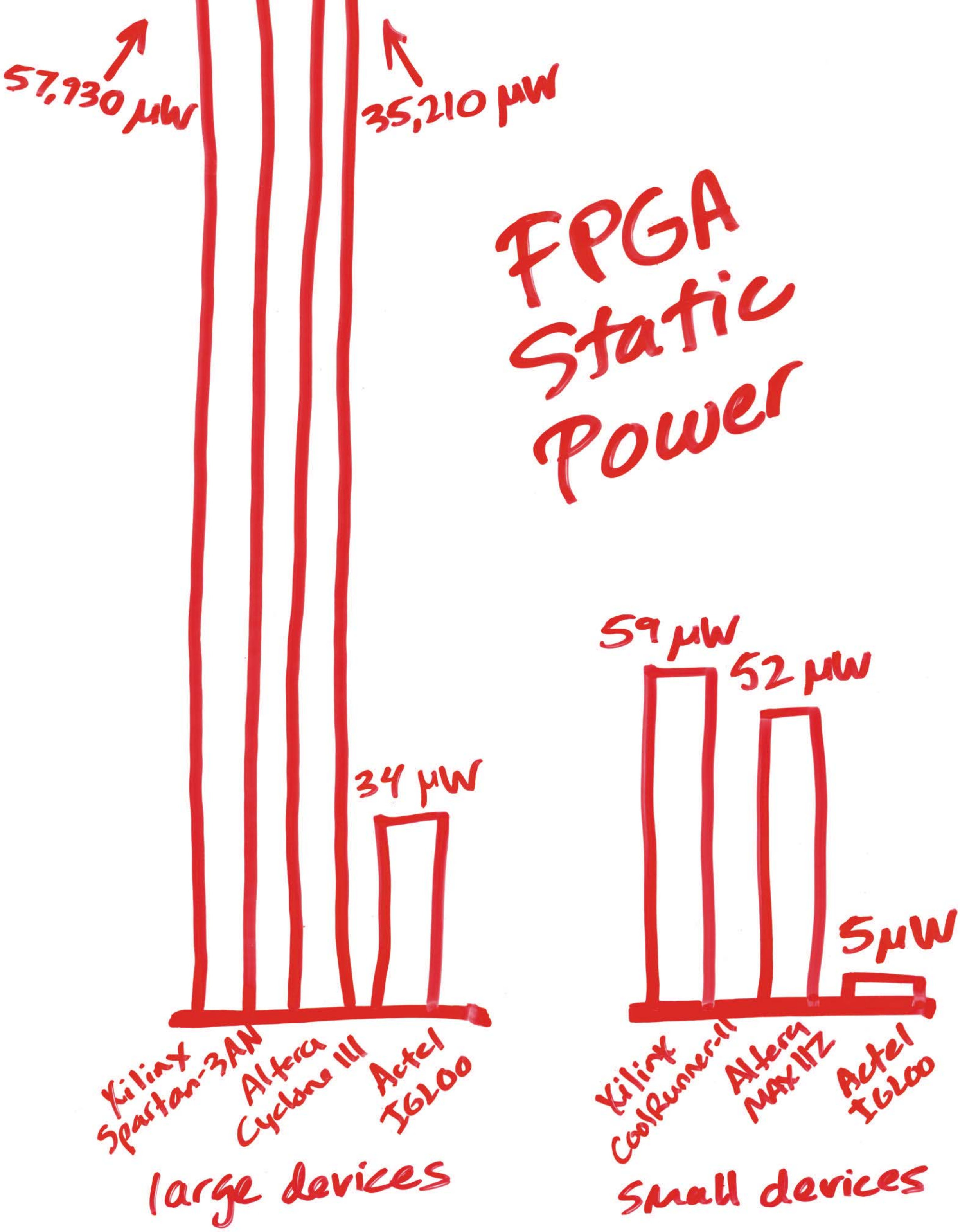


61 DC-accurate, 32-bit DAC achieves 32-bit resolution

62 Digitally programmable instrumentation amplifier offers autozeroing

64 C# application controls simple ADC

66 Perform bitwise operation in Excel spreadsheets



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contents 10.30.08

pulse

Dilbert 16

15 ESC accelerometer complies with safety standards

16 UWB IC targets handset, automotive, and industrial uses

16 A guide to SI

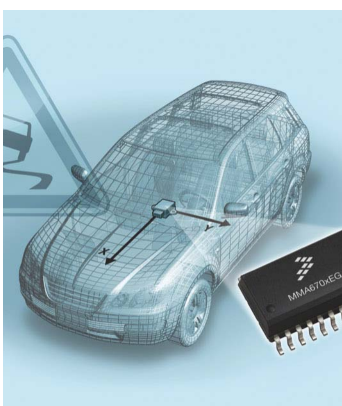
18 PSoC processors add nonvolatile SRAM to support continuous-data-logging applications

18 Industry says “no” on 450-mm wafer size but no pushback on Intel

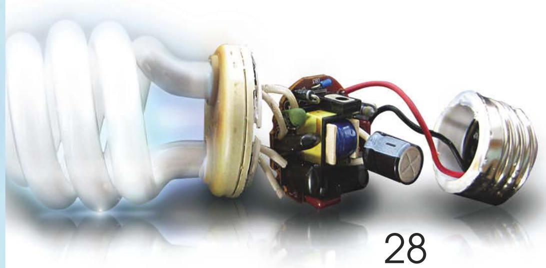
20 Gigahertz-class processor stresses energy efficiency for applications with varying usage scenarios

20 “Crystal” oscillator comes without the crystal

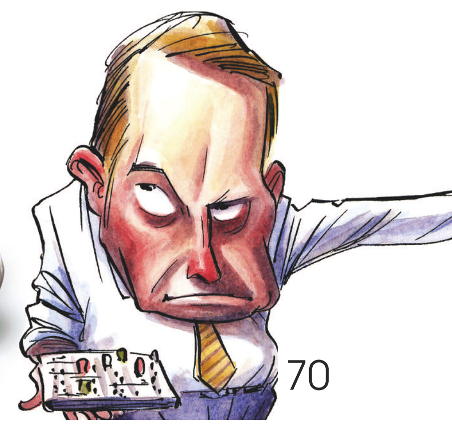
22 **Voices:** Dennis Monticelli, champion of analog innovation



15



28



70

DEPARTMENTS & COLUMNS

10 **EDN.comment:** Physics and economics

24 **Baker’s Best:** Do you question your sanity?

26 **Tapeout:** Third-party IP: placement, blocks, and clocks

28 **Prying Eyes:** Compact fluorescent lights: not always the best solution

70 **Tales from the Cube:** Stick to the schematic

PRODUCT ROUNDUP

68 **Optoelectronics/Displays:** Surface-mount LEDs and light-management ICs

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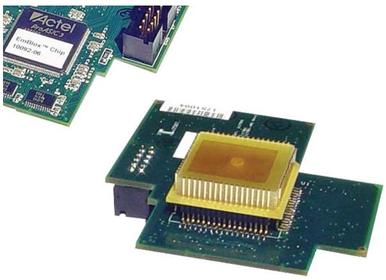

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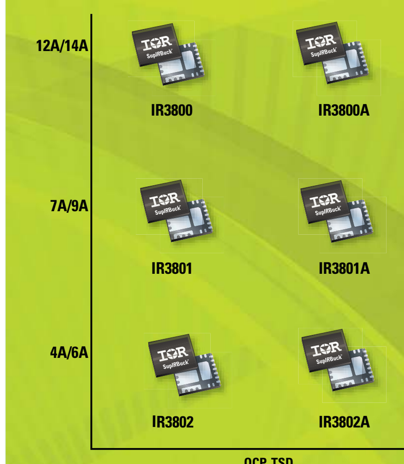

BY RICK NELSON, EDITOR-IN-CHIEF

Physics and economics

You're all aware that a relationship exists between the theories of economics and electrical engineering. As the economist Charles C Holt has written with regard to his collaboration with economist AWH Phillips on control theory, "We started corresponding in the summer of 1956 about bringing the tools of operations research and electrical engineering to bear on improving economic stability." Phillips, Holt continues, "had already published several articles applying the tools of electrical engineering to the stability of single-loop economic models," and he goes on to discuss the stabilization of economic systems incorporating multiple loops and control variables (**Reference 1**).

At press time, the economy was anything but stable, and politicians and economists have no solid proposals for stabilizing it. Economist Paul Krugman favors the US Treasury's $700 billion bailout plan, even though he says "Treasury officials have yet to offer any clear explanation of how the plan is supposed to work, probably because they themselves have no idea what they're doing" (**Reference 2**). Might engineers or scientists have some up-to-date tools to offer economists? Mark Buchanan, a theoretical physicist, says that they do but that the economists aren't listening (**Reference 3**).

Buchanan writes that part of the problem is that economists still employ traditional equilibrium theory, which holds that market values change only in response to new information. The problem, he contends, is that "a classic economic study found that, of the 50 largest single-day price movements since World War II, most happened on days when there was no significant news." And a more recent study found that news plays only a minor role in stock-price jumps (**Reference 4**). The authors report, "We find that neither idiosyncratic news nor marketwide news can explain the frequency and amplitude of price jumps."

The reason for the dissociation of price and information, Buchanan explains, is that markets have internal dynamics: "They're self-propelling systems driven in large part by what investors believe other investors believe … and traders speak for good reason of the market's optimism or pessimism."

To account for such factors, he recommends the use of "agent-based" computer models that can simulate market dynamics from the bottom up. The idea, Buchanan says, is to populate virtual markets with artificially intelligent agents who represent individuals, banks, hedge funds, regulators, and other players and to study the market behavior that emerges from the actions of the interacting agents. He cites one such model, which Yale economist John Geanakoplos and physicists Doyne Farmer and Stefan Thurner are developing. The model looks at how credit levels can influence stability. They have found, Buchanan says, although cautioning that the work remains speculative, that instability arrives suddenly, triggering "collective financial meltdown."

Unfortunately, he writes, economists are slow to adopt computer modeling, with one saying the use of computational models amounts to cheating. Buchanan adds, "This [resistance to modeling] seems decidedly peculiar given that every other branch of science from physics to molecular biology has embraced computational modeling as an invaluable tool for gaining insight into complex systems of many interacting parts, where the links between causes and effect can be tortuously convoluted."

I'd prefer that there be some computational evidence that my share of the $700 billion Wall Street bailout will actually do some good. EDN

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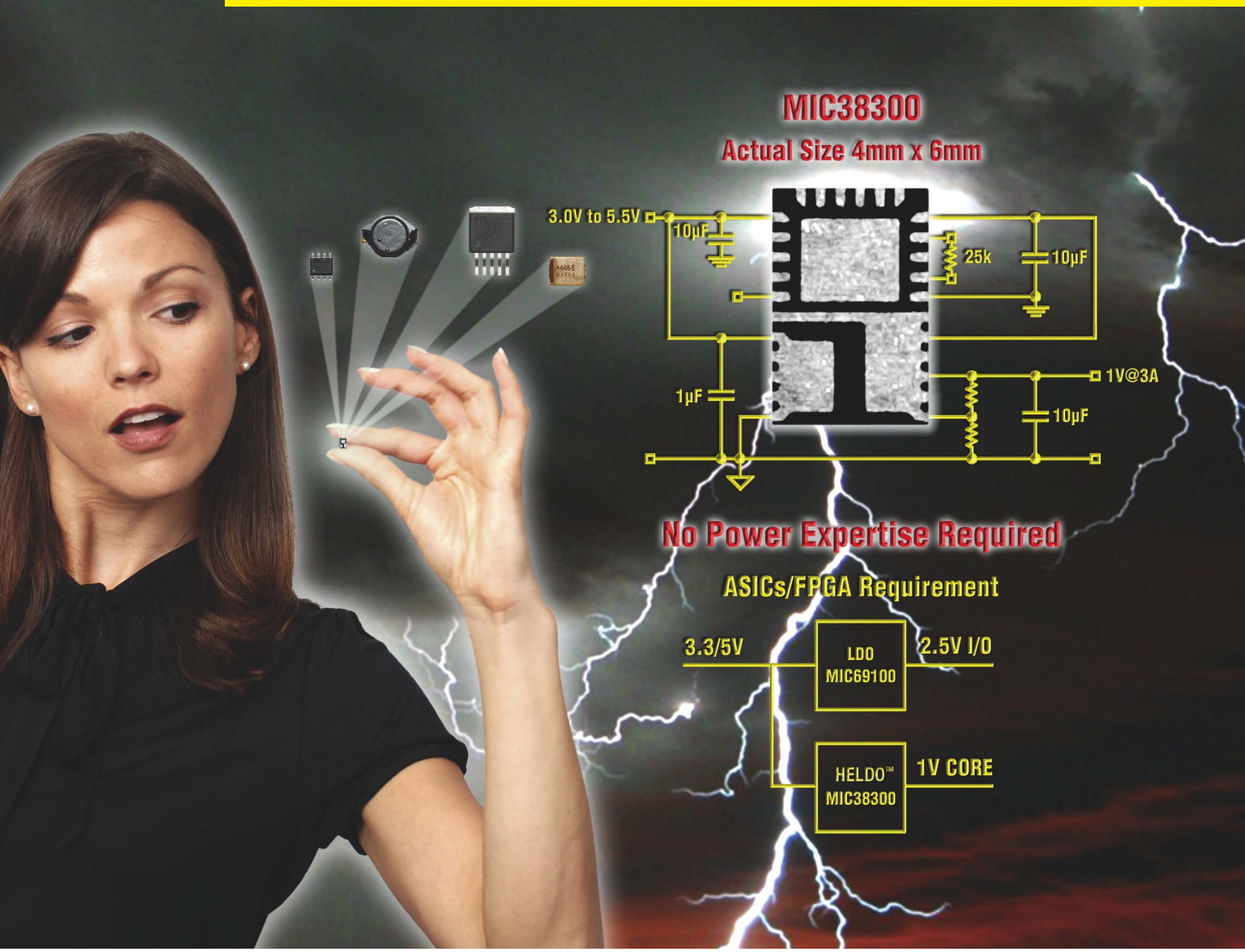

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Reed Electronics Group

ESC accelerometer complies with safety standards

ESC (electronic stability control) for automobiles is a well-established technology: In 2007, manufacturers sold more than 20 million ESC-equipped cars, accounting for approximately one-third of total auto sales. ESC's role in making cars safer led the NHTSA (National Highway Traffic Safety Administration) to require ESC systems on all passenger cars, multipurpose vehicles, trucks, and buses that automakers sell in the United States starting in model year 2012.

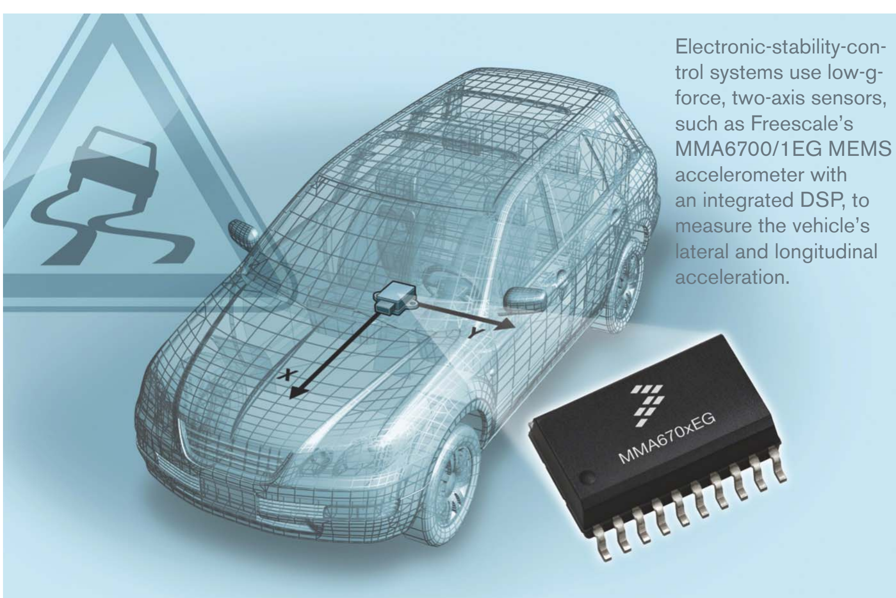
The technology relies on low-g-force, two-axis sensors to measure a vehicle's lateral and longitudinal acceleration. When these sensors detect potentially unstable driving conditions, the system sends data to the car's engine and braking system to maintain vehicle control.

Targeting ESC, Freescale's new MMA6700/1EG MEMS (microelectromechanical-system) accelerometers combine a wide dynamic range with high resolution. The devices' wide dynamic range enables the filtering of extraneous signals, such as parasitic vibrations, that could interfere with a vehicle's lateral-acceleration measurement. An integrated DSP provides support for proprietary algorithms for improved signal integrity.

The low-g sensors in an ESC system require only about 1.7 to 2g of range. The MMA6700/1EG devices provide 11 bits of accuracy and a 3.5 to 5g range to prevent the detector's electronics from saturating in extreme driving events. The sensor's bidirectional internal self-test electrostatically moves the transducer in both directions to verify sensor accuracy during the initial ignition-on test. It operates from a 3.3 or a 5V single supply and has an operating-temperature range of −40 to +125°C. The chip comes in a 20-pin-SOIC, wide-body, ROHS (restriction-of-hazardous-substances)-compliant package and sells for $7.67 (10,000).

—by Margery Conner

▷**Freescale Semiconductor**, www.freescale.com.



Electronic-stability-control systems use low-g-force, two-axis sensors, such as Freescale's MMA6700/1EG MEMS accelerometer with an integrated DSP, to measure the vehicle's lateral and longitudinal acceleration.

FEEDBACK LOOP

"When it comes to protecting your advantage in a highly competitive environment, the old adage 'there is no such thing as a free lunch' applies. Saving a few bucks on free samples at the expense of providing some salesman with a detailed explanation of your company's newest product is a risky choice at best and an expensive disaster at worst."

—Reader Bill Parrott, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6598373. Add your comments.

UWB IC targets handset, automotive, and industrial uses

Staccato Communications' second-generation UWB (ultrawideband) Ripcord2 IC integrates RF-front-end, digital-baseband, MAC (media-access-controller), and I/O functions. The single-chip, all-CMOS device covers WiMedia bands 1, 3, and 6 and has a frequency range of 3 to 9 GHz. The device uses standard 65-nm CMOS technology. The second generation moves performance forward in power consumption, size, and integration, according to the company.

The device supports multiple protocols, including wireless USB (Universal Serial Bus), high-speed Bluetooth, wireless IP (Internet Protocol), and wireless audio/video. Other features include DAA (detection and avoidance), providing a worldwide-compatible technology in a single device. Some territories and some bands—differing by country and regulatory regime—allow UWB operation only if it can detect and not transmit at the same frequency as other signals. The chip supports all time-frequency codes and data-rate modes and has USB 2.0-host/device and SDIO (secure-digital-input/output) 2.0 interfaces.

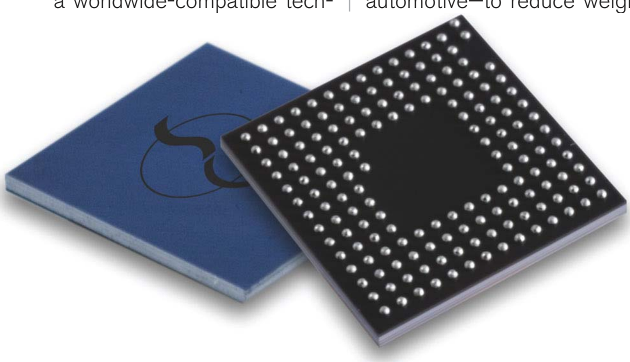
As multiple standards compete for spectrum space and—potentially—interfere with one another, UWB's ability to operate with "multiple overlapping clusters" of users will be significant, according to the company. It sees deployment in handsets—to transmit signal types, such as HD (high-definition) video—as a key direction for the technology. Other emerging applications include automotive—to reduce weight by eliminating the need for wiring—and industrial, in which the low latency for control of robotic systems might be key.

> "The Ripcord control library provides fully abstracted embedded software.

Ripcord2 also suits use in high-volume consumer applications, including handsets, DSC/DVC (digital still cameras/digital videocameras), printers, PMPs (personal media players), wireless audio/video, and mass storage. An accompanying development kit provides an IDE (integrated development environment) for native wireless-USB and high-speed-Bluetooth designs, as well as generic WiMedia UWB applications. The IDE comes with the RCL (Ripcord control library), which provides fully abstracted embedded software with portable services to simplify the interface to the Ripcord2 IC. A module incorporating the chip can occupy as little as 8.5×6 mm; the chip itself measures 5×5 mm.

—by Graham Prophet

▷**Staccato Communications**, www.staccatocommunications.com.



The single-chip, all-CMOS Ripcord2 device covers WiMedia bands 1, 3, and 6 and has a frequency range of 3 to 9 GHz.

DILBERT By Scott Adams

10.30.08

A GUIDE TO SI

The following paragraph—paraphrased from the conclusion of Chapter 1 of *A Signal Integrity Engineer's Companion* by Geoffrey Lawday, PhD; David Ireland; and Greg Edlund—summarizes what the book is about and how the authors approach their subject. Lawday teaches embedded-system design at Buckinghamshire New University (http://bucks.ac.uk) in High Wycombe, Bucks, England; Ireland is design-and-manufacturing-marketing manager for Tektronix Europe (www.tektronix.com); and Edlund is an SI (signal-integrity) expert whose résumé includes work for Cray Research (www.cray.com) and IBM (www.ibm.com). The $95, 492-pg, hardcover book (ISBN-13: 978-0-131-86006-3) is a readable treatise on a difficult subject that constantly becomes more important to designers of electronic products in the 21st century.

"The primary aim of this book is to advise you on and encourage your use of a range of best practices in the simulation, real-time test, and measurement aspects of SI engineering. For this purpose, the authors hope that you will discover how to design digitally while thinking in analog."

For the full review of this book, go to www.edn.com/article/CA6588390.

—by Dan Strassberg

▶Pearson Education/Prentice Hall, Boston, 2008, www.pearsoned.com.

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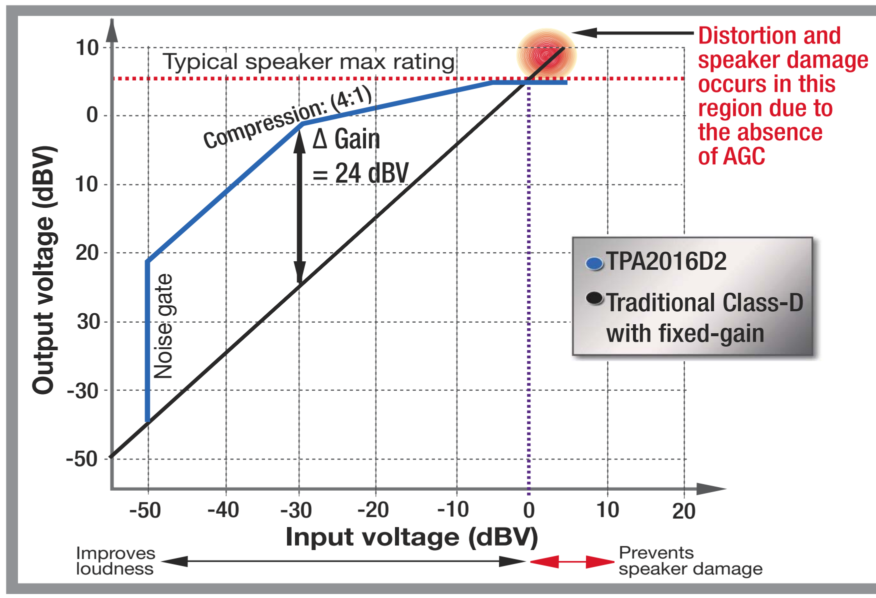
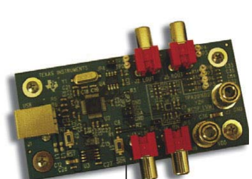


Ideal for portable applications, the **TPA2016D2** is an advanced stereo audio, Class-D amplifier. It delivers a 1.7W-per-channel output drive capability across an 8-Ω load and improves overall speaker volume compared to traditional Class-D devices. This amplifier features programmable dynamic range compression (DRC), which automatically adjusts audio levels to desired loudness ranges, protects speakers, and prevents clipping and distortion. In addition, flexible design parameters and intuitive support tools ease design and speed time-to-market.

Device	Output Power (W)	Power Supply (V) (min)	Power Supply (V) (max)	Load Impedance (Ω) (min)	PSSR (dB)	Package(s)	Price (1k)*
TPA2016D2	1.7	2.5	5.5	8	80	WCSP	$1.60
TPA2013D1	2.7	1.8	5.5	4	95	QFN, WCSP	$1.45
TPA2012D2	2.1	2.5	5.5	4	75	QFN, WCSP	$0.95
TPA203xD1	2.75	2.5	5.5	4	75	WCSP	$0.60
TPA2010D1	2.5	2.5	5.5	4	75	WCSP	$0.55

** Suggested resale price in U.S. dollars in quantities of 1,000.*



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Texas Instruments

PSoC processors add nonvolatile SRAM to support continuous-data-logging applications

Cypress Semiconductor's PSoC NV (programmable-system-on-chip/nonvolatile) family of processors integrates nonvolatile SRAM with the company's PSoC architecture. Devices in the PSoC NV family include 64 to 256 kbytes of "secure-store" nonvolatile SRAM.

Normal memory operations access an SRAM array, but the system can automatically secure the SRAM contents in a nonvolatile quantum-trap cell in case of power failure. The data transfers to and from the nonvolatile memory at speeds as high as 100 kbytes/sec. On power-up, the system can restore to SRAM the stored data at the time of power-down. The nonvolatile storage can retain data for 20 years. This type of data capture enables continuous data logging and virtually infinite endurance of the nonvolatile storage that enables field diagnostics and failure-mode analysis. To support power-down capture of the SRAM, the system design must include a 68-μF capacitor to provide enough energy to complete the data transfer.

PSoC processors include an M8C-based core that supports operating speeds as high as 24 MHz. These devices include as much as 32 kbytes of flash and 2 kbytes of SRAM. Unique to PSoC devices, as many as 12 analog blocks are available to—on the fly—create analog peripherals, such as ADC, DAC, and comparators. Additionally, the 16 digital blocks are available to create timers; counters; and PWM (pulse-width-modulator), UART, and SPI (serial-peripheral-interface) ports. The devices include an I^2C (inter-integrated-circuit) interface, watchdog and sleep timers, and an on-chip precision-voltage reference.

The 3.3V CY8CNP102B device is available for sampling now, with full production expected in the fourth quarter of this year. The device is available in a 100-pin TQFP over the industrial-temperature range of −40 to +85°C.

The PSoC NV demonstration kit and the PSoC NV evaluation kit are currently available for $100 and $55, respectively. The PSoC NV demonstration kit showcases fail-safe-data-logging capabilities in an event-monitoring and diagnostics application. It allows the device to continuously sample and log the data from multiple analog channels. The PSoC NV evaluation kit includes a fan module for temperature-sensing and fan-control applications, PSoC Designer software, and sample projects.

—by Robert Cravotta

▷**Cypress Semiconductor**, www.cypress.com.

FEEDBACK LOOP

"Until we collectively learn that productivity is only defined by adding tangible value to a product, then greed and lack of trustworthiness lead to all manner of energy wasted on sales, marketing, and legal wrangling."

—Reader Peter Kaczkowski, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6598373. Add your comments.

EDN**BLOG**

THE SANDBOX

Industry says "no" on 450-mm wafer size but no pushback on Intel

I'm starting to wonder what the real story is behind all the talk on the 450-mm wafer size. At the July Semicon West in San Francisco, "450" was the buzz, with most equipment vendors saying they won't go down that path.

SEMI (Semiconductor Equipment and Materials International, www.semi.org) recently released a report on the economics of a 450-mm wafer transition and concluded that, for now, "Shrinks, new materials, and new processes will continue to advance the industry on Moore's Law, but there are simply not enough R&D resources available to continue such advancement in nodes and processes *and* to work on a 450-mm-wafer-size transition."

This report is corroborated by a recent survey of semiconductor industry insiders by Wright Williams & Kelly Inc (www.wwk.com) that found some survey respondents did not expect to see 450-mm wafers in production until 2014 or beyond, with more than half of the respondents indicating that 450-mm wafers would never happen in production manufacturing.

After the enormous cost to make the 300-mm wafer transition, semiconductor-manufacturing-equipment vendors are rightfully cautious. However, that didn't stop Intel, Samsung, and TSMC from saying in May that they want a 450-mm wafer pilot line in 2012, justified by one Intel exec who said in July that equipment makers are overestimating the cost of moving to 450-mm wafers.

This situation seems to fly in the face of what Stanley Myers, president and chief executive officer of SEMI, said recently during a panel discussion. "Intel is *the* customer, so they are part of the analysis," referring to SEMI's report, which leads me to think that some parties are holding back what they truly think or are too shy to step up and say no to Intel, which, frankly, has called most of the shots in the equipment industry. Given the revenue-generated power and capex spending of Intel, Samsung, and TSMC combined, I'm starting to think the equipment makers may have no choice but to begin working on the move to 450 nm—whether they like it or not.

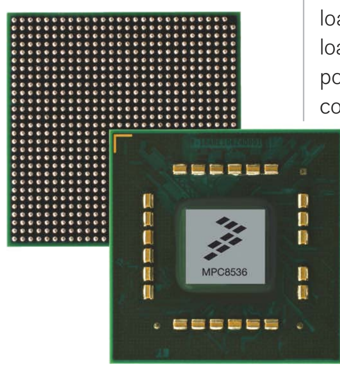
—by Ann Steffora Mutschler

▶www.edn.com/thesandbox.

▶For the full post with links, go to www.edn.com/081030b1.

Gigahertz-class processor stresses energy efficiency for applications with varying usage scenarios

Freescale's MPC8536E PowerQUICC (quad-integrated-communications-controller) III processors include advanced power- and energy-management features to support embedded media applications, such as printers and office-automation equipment, to meet environmental and governmental energy-regulatory requirements, such as Energy Star. The e500 Power processor family features the company's JOG (joint-operations-graphic) technology to maintain network traffic even when the processor is in a deep-sleep state. This energy-pacing model enables designers to leverage power states to match the workload.



The Freescale MPC8536E supports several workload scenarios to enable more efficient energy dissipation.

The devices support processing at speeds as high as 1.5 GHz for the heaviest-workload time. During light-workload periods, the devices support dynamic changes in the core frequency. The device's deep-sleep mode splits the power plane to turn off supply voltage to high-power, fast transistors in the core and cache and enable packet-lossless deep sleep and advanced Ethernet-packet filtering.

The MPC8536E includes a 512-kbyte L2 cache; an integrated security engine; 64-bit DDR2 or DDR3 scaling to a 667-MHz data rate; and a 32-bit PCI (peripheral-component-interconnect) interface, multiple PCIe (PCI Express) interfaces, enhanced local-bus-I/O interfaces, and two GbE (gigabit-Ethernet) interfaces. It also supports PCI, I^2C (inter-integrated-circuit), DUARTs (dual universal asynchronous-receiver/transmitters), and local-bus connections.

MPC8536E samples are available now, and production will begin in August 2009. The devices are software-compatible with the company's QorIQ product line. The MPC8536DS development system and the MPC8536RDK low-cost reference system in the COM Express form factor are available.**—by Robert Cravotta**
▷**Freescale Semiconductor**, www.freescale.com.

"Crystal" oscillator comes without the crystal

Silicon Laboratories is offering a new class of oscillator as a frequency reference. The all-silicon Si500 series uses neither a MEMS (microelectro-mechanical-system) frequency system nor a crystal, but it challenges crystal oscillators in the high-volume-frequency-reference sector. After you order the compensated-LC oscillators, you receive samples within two weeks with a minimum order of 75 units. The fixed-frequency devices operate at approximately 4 GHz with a factory-programmable divider chain and on-chip compensation. Silicon Labs holds stock of the unprogrammed parts and configures them to customers' orders. The company has used this strategy with crystal oscillators to match the marketing patterns with which industry buyers are familiar.

Although the initial absolute accuracy of the oscillator can be as high as 0.2 ppm, this figure is not part of the specification. The company guarantees a ±100- to ±150-ppm figure over a lifetime of 10 years—to account for aging effects—and over a temperature range of 0 to 70°C. An on-chip-compensation function predicts and compensates for drift with temperature; this correction uses both analog and digital techniques, according to the company, suggesting that the correction both shifts the oscillator's fundamental frequency and alters the digital-division ratio. Final test of the chips includes a temperature characterization that stores calibration points for each chip in the devices' nonvolatile memories.

The part, which Silicon Labs builds in 0.13-micron CMOS,

> "The Si500 uses neither a MEMS frequency system nor a crystal.

including the timing components, does not use a PLL architecture. The company describes the function that derives your specified output from the 4-GHz fundamental; you can order any frequency from 0.9 to 200 MHz as a division, but the architecture likely employs some form of synthesizer technique. A major claim for this approach is low jitter—1.5-psec-rms and maximum 2-psec/period jitter—which is comparable with crystal performance and several times better than that of MEMS technology.

The device also has high immunity to frequency change due to noise on power-supply lines. The chips drive a variety of output formats, such as CMOS, LVPECL (low-voltage positive-emitter-coupled logic), LVDS (low-voltage differential signaling), HCSL (high-speed current-steering logic), and SSTL (stub-series-terminated logic). The core oscillator uses 8 mA from 3.3, 2.5, or 1.8V; overall power dissipation depends on what you drive with it. The footprint of the plastic package is compatible with industry-standard crystal types, and you can also order a dual-output version. Expect to pay 95 cents to $2.24 (10,000).

—by Graham Prophet
▷**Silicon Labs**, www.silabs.com.

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ANALOG DEVICES

VOICES

Dennis Monticelli, champion of analog innovation

Dennis M Monticelli in 1974 received his bachelor's degree in electrical engineering from the University of California—Santa Barbara and joined National Semiconductor Corp upon graduation. In 2000, he became a National fellow. Monticelli currently serves as chief technologist for the company's analog-products group. He holds 20 patents in circuit design. *EDN* recently had the chance to interview Monticelli. A portion of that interview follows. To read more, go to www.edn.com/081030pulse1.

Do you see foreign engineers as less innovative?

A The ability to innovate has nothing to do with DNA, but culture definitely plays a role. Some cultures encourage risk taking and thinking differently from the pack more so than others. If a global company creates a strong internal culture of innovation, it will supersede any differences among foreign cultures with regard to fostering innovation.

What can a company do to foster global innovation?

A Build a strong internal culture that values innovation. The innovation subculture has to permeate the company's overall culture and be closely coupled to the entire risk/reward system. There also has to be a specific infrastructure to support it in the form of allowing personal time apart from day-to-day work and a separate budget for research and experimentation. It needs to be OK to fail within that infrastructure. You openly celebrate the wins, which are probably well less than 50%, and reap useful lessons from the failures.

Is innovation primarily a collaborative effort?

A It is a collaborative effort because it is now a bigger industry and there are so many players. Nowadays, we are large, diversified, and worldwide, so companies need a process for innovation so they can engage as many people as possible.

Is it harder to do analog innovation?

A Analog has more variables associated with it, and that [fact] permeates the way you deal with it. It is just not as deterministic as digital. You can break up something deterministic into its constituent tasks and execute each one and get to the finish line. With analog, there are so many variables you need to do things a little differently, particularly with the innovation process where there is inherently risk involved. There will be failure. There should be failure. You have to find a way to accommodate the failure in positive ways so you don't discourage people. Companies, without realizing it, will sock you if you fail. That's why you need to create

a subculture of innovation that says "OK, in a percentage of my time or resources, I can do this [task]; it's OK to fail within that bucket. If I fail, even utterly, I don't tank the company." You are expected to succeed a percentage of the time ... everyone understands it is a minority of the time you come up with something good, but the upside is great when you do. It doesn't have to be a technical innovation; there is plenty of opportunity for innovation all through the business.

Does the lack of effective IP (intellectual-property) protection in China make innovation better or worse?

A It is very difficult to protect both patented IP and trade secrets within China. It will get better over time as China learns to value its own IP, but, for now, wisdom dictates that sensitive IP should not go there, and yes, this [belief] constrains the innovation potential of that region on behalf of the global company.

Is it worth it to take out worldwide patents?

A Yes, it is worth it to take out worldwide patents, but it should be determined on a case-by-case basis. Protection of IP in the worldwide court systems is OK, except for areas of the developing world where IP is simply not highly valued yet. By the way, there is no patent system in the world that gets an A on my report card, and most struggle to earn a B.

What is the secret to your record of innovation?

A I'm pleased to say that there is a whole list of talented engineers and scientists at National who have passed me by in the patent count. But there is no great secret to it—just an ability to identify promising new areas and a willingness to commit myself to attacking the most challenging technical problems in those new areas. Out of that foundation comes the opportunity to make useful inventions.

Is it harder to find analog talent overseas?

A Yes and no. In years back, it was easier to find analog people in Europe. The United States went through a period in the late 1980s and most of the '90s where we were distracted by the PC platform, and curricula swung over to digital. Analog wasn't being taught. In Europe, it was automotive, telecom, and industrial, and all those have a higher analog content than PCs. The wireless revolution turned it around in the United States. That [revolution is] what made analog fashionable again. From there, we started getting broader analog curricula—not just the RF—so, right now, the US schools are in pretty good shape. If you go to Asia, you find a definite falloff in analog- and mixed-signal capability. There is some advanced stuff going on out there, but analog- and mixed-signal [technology] is not well-developed. There are little oases of activity here and there, but it's not a place where you would want to set up a major research effort.

—Interview conducted and edited by Paul Rako

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ANALOG DEVICES

BY BONNIE BAKER

Do you question your sanity?

Have you ever been in need of a second opinion when your sanity is at stake? The pulse oximeter may be able to provide that second opinion if your brain is oxygen-deprived. This condition could affect you if you are a pilot, hiking in the high altitude of a mountain range, or even undergoing surgery. The pulse oximeter is a noninvasive instrument that monitors SpO_2 (saturation of hemoglobin with oxygen) in your blood.

You measure the oxygen in the blood by alternating the on-times of a red LED with a 650-mm wavelength and an NIR (near-infrared) LED with a 940-mm wavelength, taking the ratio between the intensities from a photodiode, and comparing that ratio with an SpO_2 look-up table in the microcontroller (**Reference 1**).

The transimpedance amplifier appears in medical and laboratory instrumentation, position and proximity sensors, photographic analyzers, bar-code scanners, and even smoke detectors. In the medical field, you will primarily find transimpedance amplifiers in the CT (computed-tomography)-scanner front end and the pulse oximeter. **Figure 1** shows a simplified block diagram of a pulse oximeter (**Reference 2**).

In the circuit in **Figure 1**, the red LED is on for 50 µsec, both LEDs are off for 450 µsec, the NIR LED is on for 50 µsec, and then both LEDs are off for 450 µsec. The system repeats this cycle continuously. The transimpedance amplifier, A_1, converts the photodiode current generated by the LEDs to a voltage at the output. The signal then travels through a bandpass filter and gain stage to the 12-bit ADC. The signal also travels through a lowpass filter to regulate the driver power to the LEDs. The microcontroller acquires the signals from the 12-bit ADC, computes the ratio of the red- and NIR-LED signals, and compares the results with a look-up table. The LCD shows a percentage of oxygenated hemoglobin versus nonoxygenated hemoglobin and your heart rate.

When you choose your device for the pulse-oximeter transimpedance-amplifier circuit, you need to make sure that the amplifier's input-bias current is very low or in a picoamp region at 25°C. The amplifier's input-bias current creates an output-voltage error by conducting through the high-impedance resistor, R_F, in the amplifier's feedback loop. FET- or CMOS-amplifier input devices usually meet this requirement. A second consideration is that the low-frequency voltage noise of your amplifier must be very low. When you consider the input-voltage noise of the amplifier, scrutinize the impact of the flicker noise. After the transimpedance amplifier, a bandpass filter eliminates the noise above 5 Hz. Finally, the amplifier's initial offset error and overtemperature should be in the microvolt region if you want to minimize linearity errors. It may be worthwhile to use an autozero amplifier.

A normal output for the pulse oximeter is approximately 97%±2%, ranging from 95 to 100%. The alarms on the pulse oximeter usually sound when the SpO_2 level drops below 90%. If there is a shortage of oxygen in your system, you may experience poor judgment or loss of motor function. If a pulse oximeter indicates that your oxygen levels are stable, you may want to explore other diagnostic avenues, or perhaps you just dance to the beat of a different drummer. Good luck! **EDN**

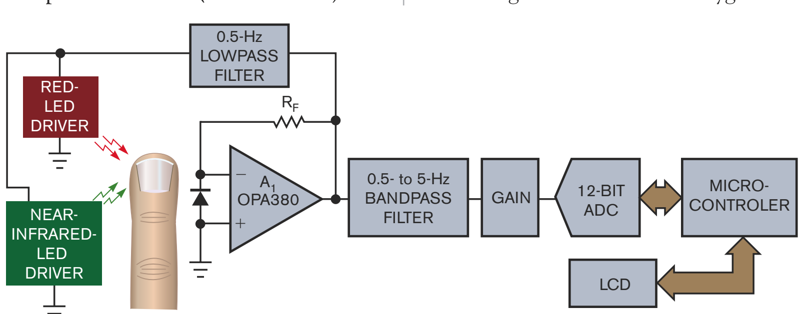

Figure 1 This pulse-oximeter circuit alternates the on-time of a red LED and a near-infrared LED to monitor oxygen saturation in the blood.

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BY PALLAB CHATTERJEE, CONTRIBUTING TECHNICAL EDITOR

Third-party IP: placement, blocks, and clocks

In the last few columns, I have discussed questions you should ask your IP (intellectual-property) providers before launching into a new design (**references 1** through **4**). Wrapping up this topic, I'd like to discuss some questions regarding placement, rotation, embedded blocks, and clocks. These issues pertain to both hard and soft IP and have to do with some of the overall design issues in the construction and method for the SOC (system on chip) you are creating.

Most SOC designers organize the floorplan by minimizing the layout of the data bus. The key is to ensure that you optimally place and orient the pins for the blocks so that the data bus can flow with the fewest bends, branches, and changes in symmetry. Clearly, placement of the IP has implications for this pin connectivity, as well as for routing congestion, timing performance, and power consumption.

Unfortunately, some automatic-placement programs work from the physical data and pin-congestion data and do not necessarily place the same priority on timing and power constraints. So, designers have some decisions to make. Providers of soft IP must identify whether the block must be a single contiguous piece or whether the designer is free to distribute it as necessary to optimize pin locations. For hard IP, the designer must deal with the issues of placement orientation: rotation and reflection.

In some cases, such as with memory blocks, the timing and IR (current/resistance) drop for two instances of the same block may match only if you place both blocks on the same thermal plane and in the same orientation. Datapath blocks and most high-speed RAMs are sensitive to orientation, which can affect their performance on both an absolute and a relative basis. For that reason, the IP provider must provide guidelines about how to position such blocks in the SOC and what sort of blocks a designer may safely locate nearby.

If an IP vendor can't answer some basic questions, the blocks may not be robust and may have a questionable origin.

Placing embedded blocks inside other IP blocks is also an issue. Soft IP for a megacell may consider instances of hard IP in other parts of the chip as stand-alone blocks. So, IP providers must identify within their IP any unique parameters associated with the design and physical-implementation issue of the embedded block and differentiate them from stand-alone applications in the same block.

Designers must also consider clocks because clock designs are as diverse as the types of SOCs that use them. Most companies have their own "hybrid" methods, which mix their preferred design styles with the trade-offs necessary for working with the design tools they have chosen. Third-party IP must conform to either the design tools or the styles in use because both typically differ from what the IP developer used originally to make the block.

So, the design team needs some more information. Should a designer extend the clocks inside the block or only to the top-level pins? If the clocks go inside the block, should the designer structure them hierarchically or place them flat at the top level and connect them in a "local-global" fashion to the buried pins inside? Is there a preferred clock-tree shape for reaching the block?

Designers also need to address many design- and process-specific questions. If an IP vendor can't answer some basic questions, the blocks may not be robust and may have a questionable origin. Even if the IP vendor has answers, the interpretation of the answers and how those answers affect and apply to your design are issues that you must work out for yourself.EDN

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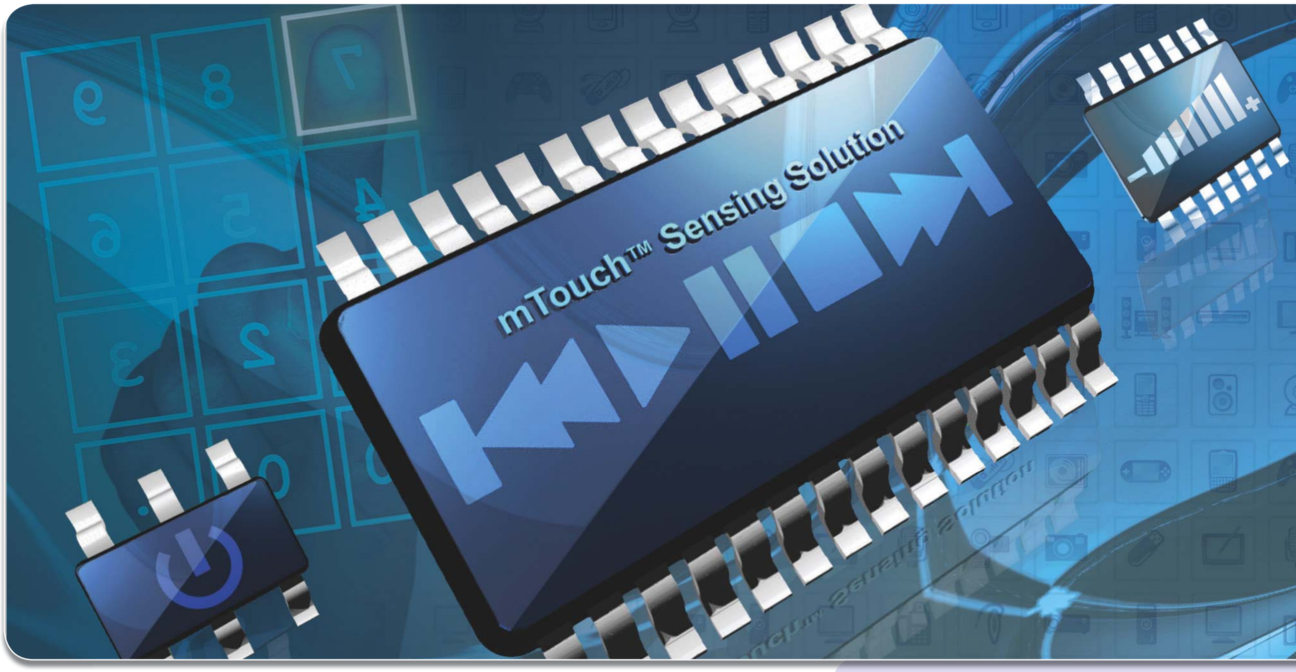
Capacitive Touch Sensing In a Flexible, Single-chip Solution



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THE mTouch SENSING SOLUTION FEATURES:

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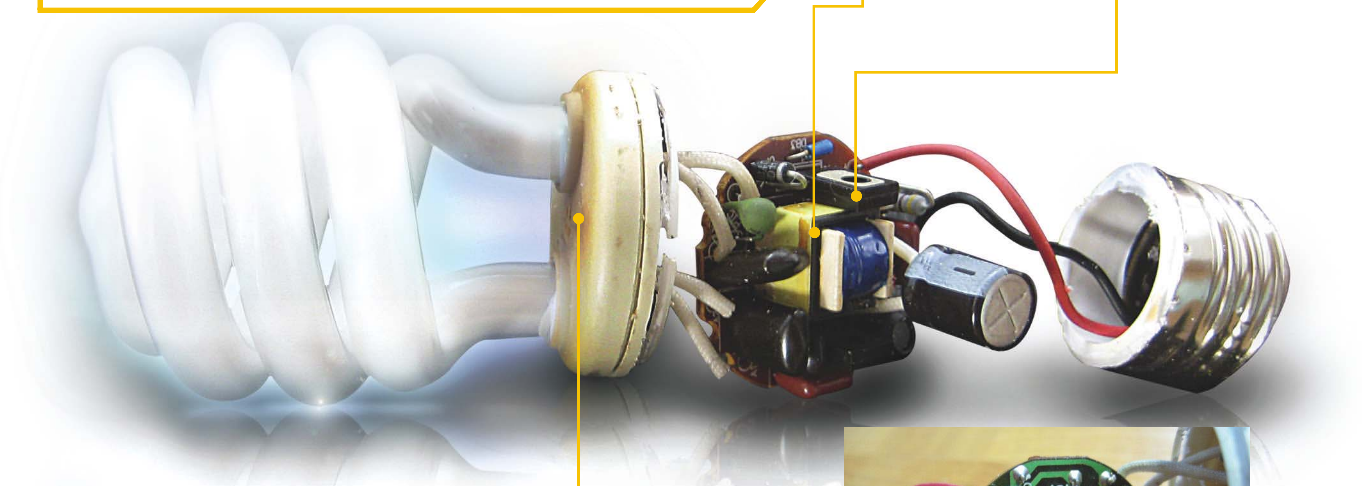
Compact fluorescent lights: not always the best solution

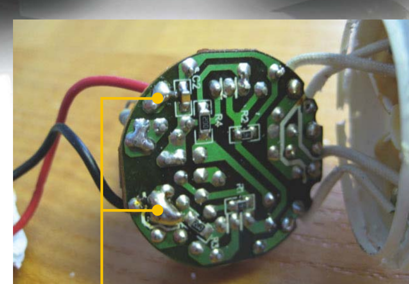
After mentioning in a PowerSource blog post my difficulties with CFLs (compact fluorescent lights) and their tendency to burn out after less than a year of use, I was surprised by the number of comments I received from irate CFL users with similar experiences. It turns out that the lights are not the universal panaceas their developers claimed they would be as replacements for the venerable incandescent light bulbs.

The ideal use for a CFL is in lighting fixtures, such as table lamps, in which the screw-in end is below the unconfined bulb. Sure enough, all but one of my dead CFLs came from enclosed downward-pointing lights with the screw-in end above the heat-generating bulb. In fact, in the whole house, I counted just three upward-pointing, unenclosed lights that would be appropriate for CFLs. Energy Star's Web site, www.energystar.gov, states that "CFLs perform best in open fixtures that allow airflow, such as table and floor lamps, wall sconces, pendants, and outdoor fixtures" (see www.energystar.gov/index.cfm?c5cfls.pr_cfls). The Web site also recommends installing CFLs in fixtures that you use at least 15 minutes at a time or several hours per day, which excludes such areas as closets and laundry rooms.

Like any other fluorescent light, a CFL is a gas-discharge tube. It relies on an inductor acting as a ballast to limit the ac current through the tube.

Because the inductor would have to be unreasonably large if the CFL operated at the line frequency of 60 Hz, the CFL's circuitry includes a frequency-multiplier stage relying on several high-voltage transistors; this stage allows for the use of a smaller inductor and smaller current, as well.

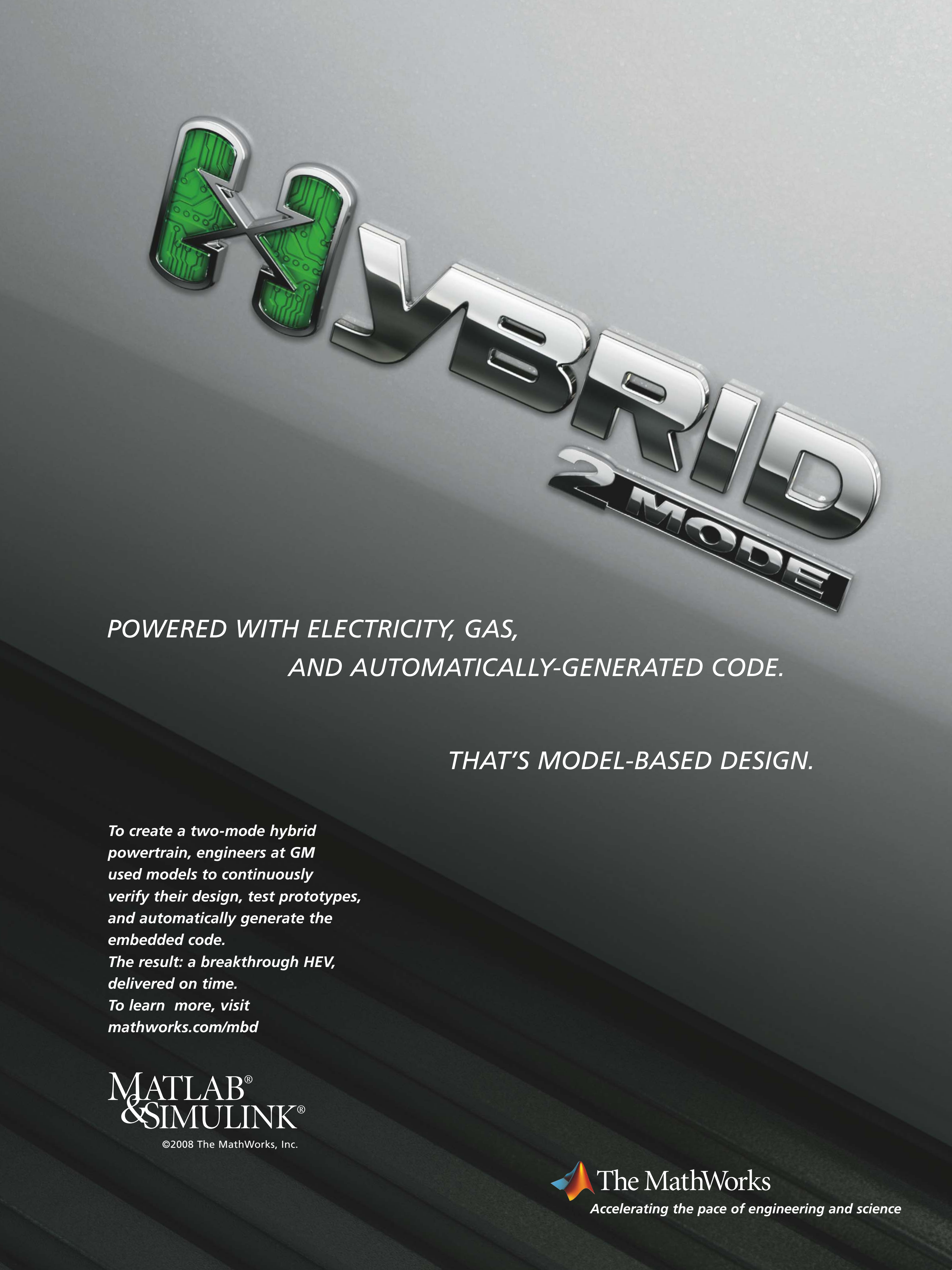




Using an infrared-thermometer gun, I found that the CFL in an enclosed, downward-facing configuration yielded a temperature of 160°F, 40 degrees higher than the table-lamp CFL's temperature of 120°F and a significant difference that can shorten the bulb's life.

Compared with an incandescent bulb, a CFL is crammed with electronics. Note the telltale brown stains at the base of the bulb where the CFL overheated.

Note the significant amount of hand assembly a CFL requires, both increasing cost and decreasing reliability. All of the wires require hand assembly and soldering.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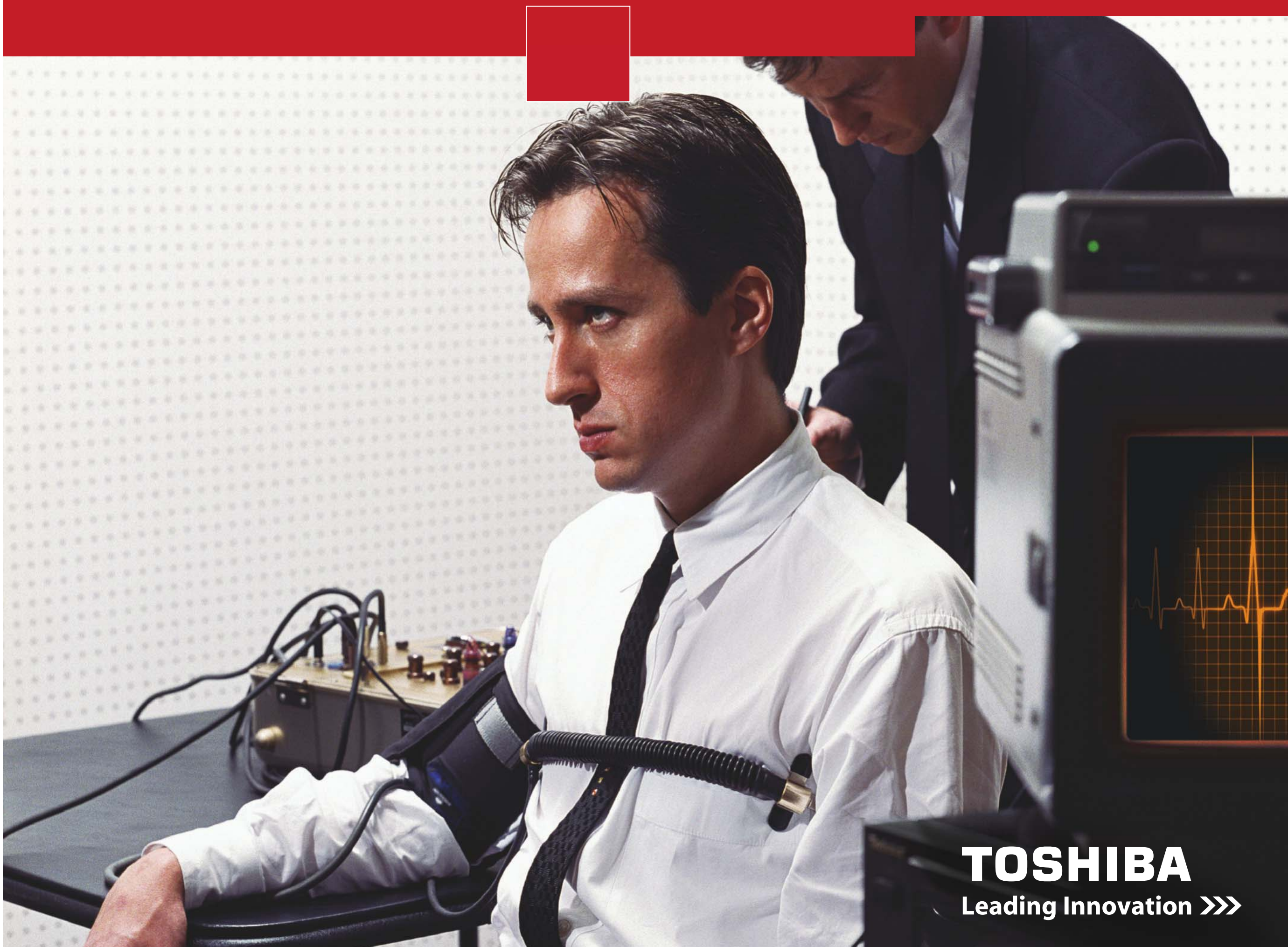


WILL SYSTEMS ON CHIPS FOLLOW SERVER CPUs DOWN THE ROAD TO HAVING MANY IDENTICAL PROCESSOR CORES ON A DIE?

BY RON WILSON • EXECUTIVE EDITOR

Multicore: the future of SOCs?

From the early days of SOCs (systems on chips), when the devices were simply single-chip integrations of board-level microcomputers, their architectural evolution has followed a single clear path. Architects added memory. They integrated application accelerators to execute specific, clearly defined tasks with greater speed and less energy. They introduced more complex interconnect structures and DRAM controllers to support data flows among the blocks.

Then, Intel announced a change of direction in the server market. Under pressure from the realities of less-than-100-nm processes, Intel shifted its focus from ever-faster CPUs to multiple simpler CPUs on one die. This new way to use the transistor budget delivered Intel from the futile search for greater instruction-level parallelism and saved it from the growing energy cost of higher clock frequencies. It also fit the needs of the server world, in which job mixes often present a rich pool of independent threads to execute on the multiple cores.

Today, some SOC architects view the multicore movement as irrelevant to the embedded, often hard-real-time world of SOCs. But others predict that as we move from 90 nm to 65 and 45 nm and beyond, SOCs will follow server and PC-processor chips into the multicore world. Instead of today's typical architecture, in which a single CPU core sits at the center of a complex fabric of buses and controls a heterogeneous collection of specialized engines and peripherals, a multicore SOC might look more like a sea of nearly identical CPU cores. Perhaps there would be a few application-specific processor cores, as well, and certainly, there would be a huge portion of on-chip memory—some local to the processor cores and some shared. But in contrast with today's SOCs, there likely would not be a single controlling processor. Rather, the system would distribute control among the cores, and this distributed kernel would dynamically map tasks onto cores, according to current needs and power constraints.

It sounds radical. But examples now exist of SOCs moving in this direction. If the vision comes to pass, it will change much of today's conventional wisdom about SOCs and how they work.

THE MOTIVATION

Why would architects contemplate such a radical change? There are two primary reasons: The first is power, and the second is scalability.

In principle, the attraction of multicore processing for power reduction is compelling. By splitting a set of tasks among multiple processor cores, you reduce the operating frequency necessary for each core, allowing you to reduce the voltage on each core. Because dynamic power is proportional to the frequency and to the square of the voltage, you get a big gain there, even though you may have more cores running. Even static power improves as you turn down supply voltage.

Clever software can take even better advantage of the situation. "In the ARM architecture, the wait-for-interrupt instruction gates the CPU clocks, so you pay dynamic power only for cores that are actually doing something," notes ARM's product manager, Ian Rickards. "And Linux is capable of recognizing when a core is not being used at all and powering it down altogether. An extension of this idea—which I haven't seen used yet in multicore configurations—is to use dynamic-voltage-frequency scaling, so that the operating system keeps each core running at the minimum voltage and frequency necessary for its current task."

Rickards points out that there are other power gains from the lower frequency. If the cores require a lower maximum frequency, it may be possible to use, for example, an LP process instead of a G process or to use 10-track libraries instead of high-performance, 12-track libraries. All of these gains add up to big savings.

But architects have to weigh these advantages against the inherent energy inefficiencies of a programmed-instruction machine compared with those of a hardwired engine. "Accelerators will always be better on power consumption, especially on well-defined tasks like security calculations or regular-expression matching, where the Harvard architecture is nonoptimal," observes Dan Bouvier, chief technology officer of the microprocessor division of AMCC (Applied Micro Circuits Corp). The simple fact that a programmed architecture has to fetch and decode instructions—whereas a state machine does not—creates a difference in energy consumption. And general-purpose processors often must use many instructions to accomplish what dedicated hardware can do in a single cycle. Skilled power management and custom instruction hardware can minimize these differences but can't entirely erase them, especially if you compare a power-optimized CPU core with a dedicated engine that is just as optimized.

AT A GLANCE

- SOCs (systems on chips) are evolving from CPU-centric to multicore architectures.
- SOCs' evolution presents significant power and scaling advantages.
- Multicore SOCs present many issues unfamiliar to most SOC-design teams.
- Debugging may be the largest single challenge.

As the number of processor cores in the SOC increases, the second factor, scalability, becomes important, as well. "It's much easier to scale with a uniform architecture," Bouvier says. "If you use specialized accelerators, the non-uniform-programming model creates havoc."

Vamsi Boppana, senior director of technology at Open-Silicon, makes the same point from a hardware architect's point of view. "I'm a huge believer that we are at an inflection point," Boppana says. "We are seeing designs go through now with several hundred processors on a die. It won't be long until there are thousands. With that many processors, there is simply no way you could manage the complexity of a heterogeneous architecture with static task assignments. These architectures must use SMP [symmetric multiprocessing]."

CREATING THE ARCHITECTURE

In the view of these experts, then, the future of SOCs lies in more uniform arrays of general-purpose processors. But how do we get from today's heterogeneous, statically mapped, CPU-centric designs to those SMP designs? The answer is to go back to the application.

"You start out by looking at the nature of the parallelism the application presents, and the nature of the problem you are trying to solve," states Tensilica's Chief Technology Officer Chris Rowen. "At the first order, there is usually a fair amount of parallelism between the different functional subsystems in an SOC. For instance, the layers of the protocol stack and the video processing in an Internet Protocol set-top box can run pretty independently. You see a lot of that kind of potential parallelism in the data plane. It's a historical artifact from the days when the functions were separate chips.

"That kind of structure gives you a start on spreading an application across multiple processor cores. The hard part is teasing apart the single big, unpipelined tasks that are left after you have done the easy part."

Rowen says that, at the next level of complexity, creating the infrastructure

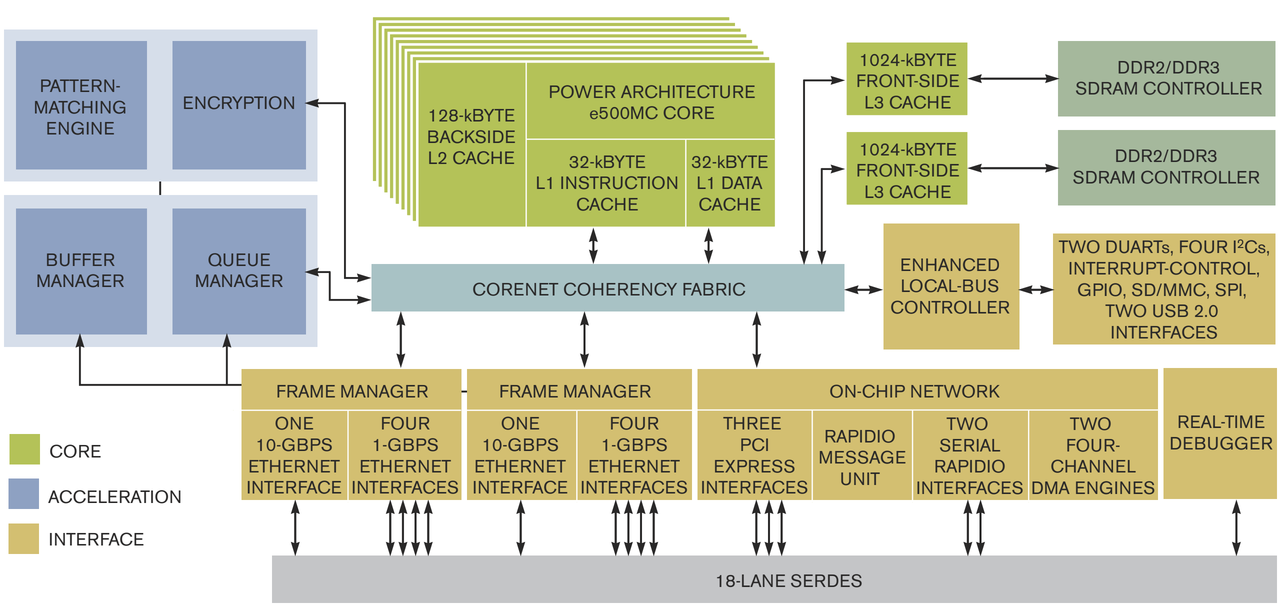


Figure 1 An eight-processor, multicore SOC, the Freescale P4080, illustrates the evolution of SOCs away from a single CPU with hardware accelerators.

in which the processor cores operate is equally important. As you divide tasks into separate threads, he says, you will see two categories of the connections between the tasks: data-streaming connections, in which data flows in an ordered way from one task into the other, and complex, shared-data connections, in which the exchange of data is unordered and possibly unpredictable. For these two situations, you need two kinds of connections between the processors: queued interconnect for the data streams and combinations of shared-memory, interprocessor-communications mechanisms and programming models for the more complex situations.

THE INTERCONNECT

As the processing elements in the SOC become more nearly identical, the question of interconnect and memory architectures becomes more pressing. There is a natural tension here between wanting to keep the array of processors completely symmetric so that the operating-system kernel can move tasks around at will and needing to have specific kinds of interconnections for specific kinds of data sharing.

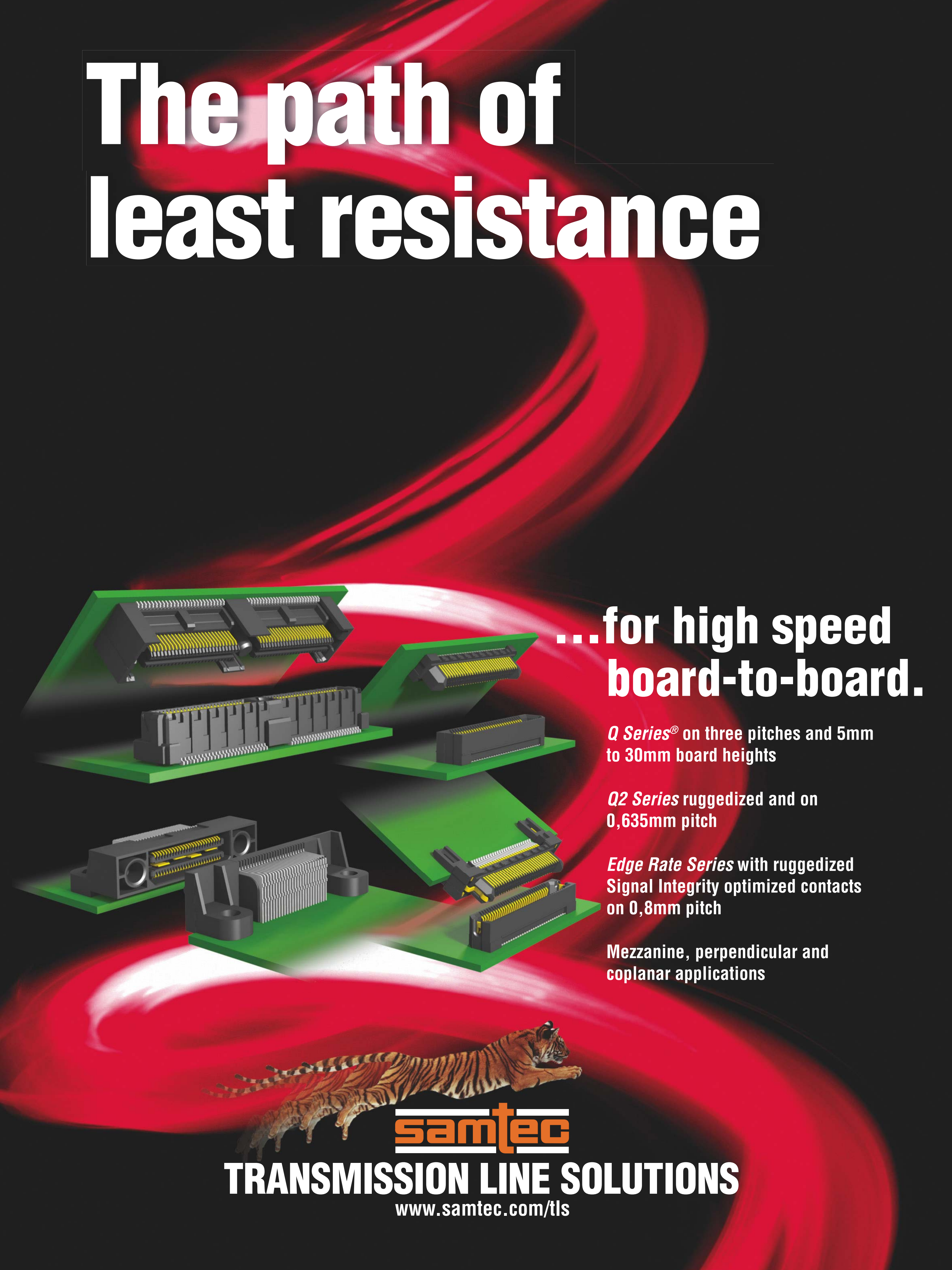
The simplest approach to this problem is to emulate the server world: Give all the processors local caches, often private at L1 and L2, sitting above a huge shared memory (**Figure 1**). In this way, the programming model is that all the processors always have access to all the memory.

Most architects are adamant that such an approach must have full hardware-supported coherency. "The minimum hardware configuration would include cache coherency across all the processors," says Kerry Johnson, director of product management at QNX Software Systems. Although it is possible to run a system without hardware coherency, most feel it is simply too complex a problem and shifts too much overhead to the software.

But shared memory may not be the only logical connection between the processors. AMCC's Bouvier suggests that the interconnect may also want to support some form of hardware-based message-passing or other direct interprocessor-communications link, as well as hardware for I/O virtualization, so that when the system assigns a task to a new processor, the processor doesn't lose its connection to its I/O streams. The ability to move operating-system tasks, rather than keep them static, also means that you need to either centralize or uniformly distribute interrupt-control and DMA (direct-memory-access) hardware to maintain symmetry.

So, how does the hardware team implement all these facilities without creating too much overhead? That question is nontrivial. Even just connecting the local caches to the shared memory has proved challenging, driving designers from traditional shared buses to switch-based interconnect to complex multilevel interconnect. Adding the need for direct messaging between processors just makes the problem more interesting.

"One of the key questions is how you feed all the engines while staying within your power envelope," says Dac Pham, director of platforms at Freescale Semiconductor. "You have to look at both the bandwidth and the latency needs of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individual data flows, or you can end up starving your CPUs."

"The solution is not just one approach or the other," adds Freescale Senior Systems Architect Steve Cole. "For instance, in a recent design, we have employed three levels of cache, a switch-based interconnect, and a configurable hardware-coherency system that allows the designer to extend coherency over some memory structures but not others. It's important to let the designer avoid the power and latency hits where he doesn't need coherency, such as in simple flow-through data movement in the data plane," explains Pham.

UNSOLVED PROBLEMS

Clearly, there is a road map from today's SOCs to symmetric-multicore SOCs. But there are also unsolved problems along the way. Chief among these issues are finding enough parallelism in the application to use all those processors, dealing with hard-real-time constraints, finding a distributed operating system to work in this environment, and debugging the resulting system.

Creating parallelism is a necessary first step in exploiting multicore designs. If the parallelism comes from innate data parallelism—for instance, the nearly independent processing of macroblocks in video compression—then the problem may be relatively easy. If finding parallelism requires finding independent program threads in existing algorithms, however, the problem has no known analytical solution; it takes hard work, genius, and luck in about equal measures.

"The embedded world will develop multithreaded applications," insists Cole. "But, more often than not, the code will be developed from scratch or acquired from a start-up, not developed by reworking existing single-threaded code."

Real-time constraints are other sticking points. Cache-coherent symmetric-multiprocessing systems are inherently nondeterministic because you cannot predict the latency on a load operation without knowing the exact origin of the data. In a system with dynamic task allocation, the response to an interrupt can vary wildly depending on the task mapping and state of the processors—and their power management—at the instant the interrupt is decoded. The Microsoft approach of declaring a nondeterministic system to be real-time if it runs fast enough may prove inadequate in the SOC world.

These facts lead some architects to believe that there will always be a firm partition between the symmetric and the real-time portions of the hardware, with real-time tasks statically mapped onto specialized processors outside the symmetric-multicore array. "I think you will see processors cluster together," Bouvier says, "with some processors grouping as an SMP subsystem and others standing alone and running their own instances of a real-time operating system."

Just where the operating system goes is another work in progress. Many architects believe that bringing SMP into the SOC world will eventually require a genuine distributed operating system, in which there is no one master instance of the kernel running on a particular processor but rather a microkernel on each processor with the system dynamically allocating all the other operating-system threads to processors. Embedded-Linux designers are working to accomplish this goal, but no one yet points to a finished product.

Finally, there is the huge matter of debugging. "Distributed applications will require a totally different way of debugging," says Open-Silicon's Boppana. "They need a consistent way to access and probe an application and a reliable way of replaying how things actually happened leading up to an event. And people are asking for more kinds of information, as well—activity monitors and thermal monitors, for instance. There is a lot of research going on in this area now."

Bouvier agrees. "As we move from one big fat thread to many finer threads, the number of interprocessor dependencies grows. This situation creates a real debugging challenge: How do you run, stop, or trace a multiprocessor system with these dependencies? If you can capture this much data, how do you get it out of the chip?" he asks.

Despite these issues, some SOCs today already employ regions of symmetric-multicore processing. In some applications with a high degree of parallelism, such as network processing, the trend has already advanced to large numbers of processors and threads. And it seems clear that this evolution will continue and spread. As it does, much of the complexity that today resides in the hardware architecture and implementation will move into the software, changing the makeup of an SOC design team. **EDN**

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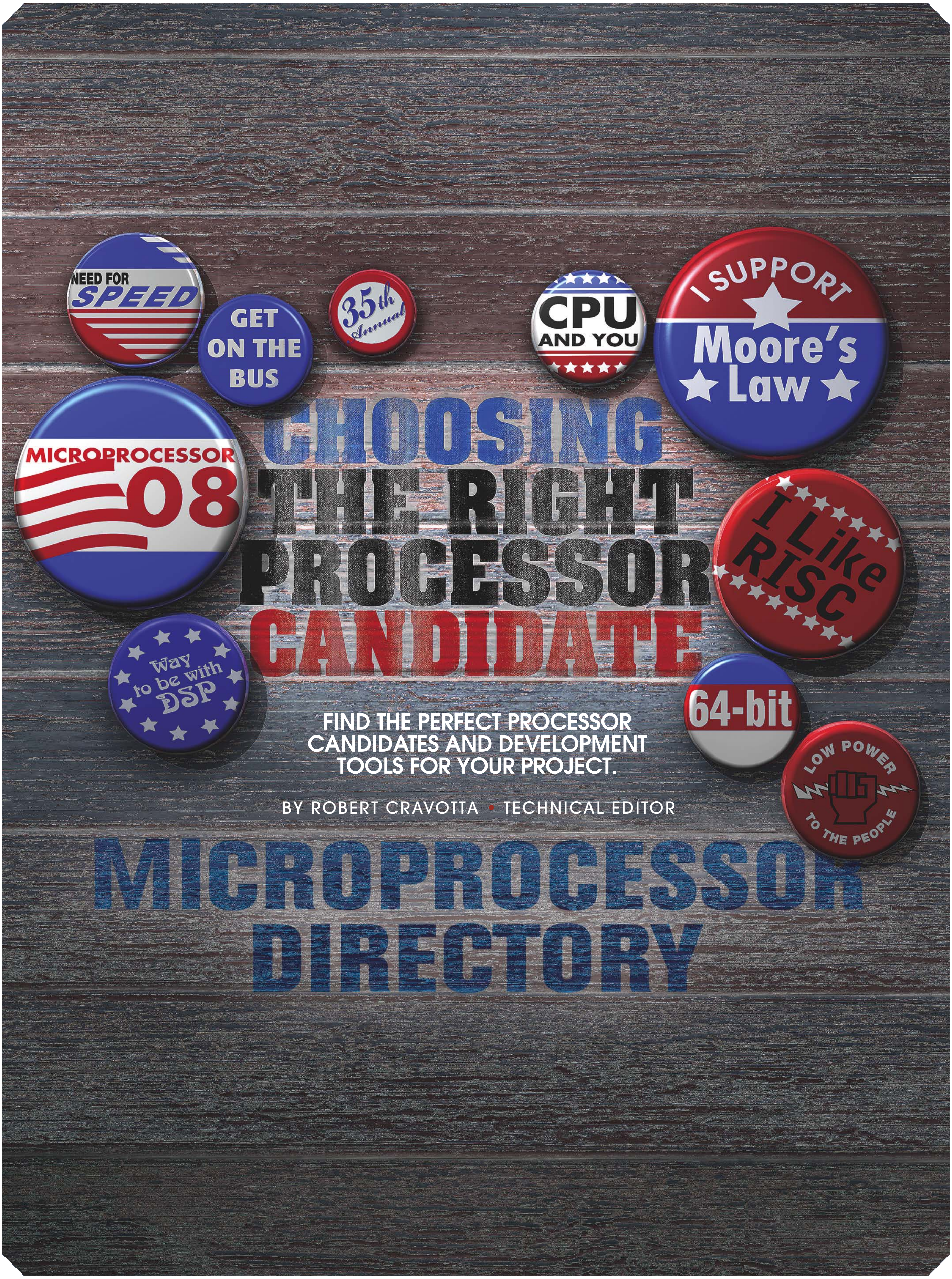

CHOOSING THE RIGHT PROCESSOR CANDIDATE

FIND THE PERFECT PROCESSOR CANDIDATES AND DEVELOPMENT TOOLS FOR YOUR PROJECT.

BY ROBERT CRAVOTTA • TECHNICAL EDITOR

MICROPROCESSOR DIRECTORY

Welcome to the 35th annual *EDN* microprocessor/microcontroller directory. Once again, the companies and devices in the directory continue to evolve and grow in number. The company roster and product listings are testaments to the variety of processors available and the tremendous variation among requirements, features, and types of applications for which designers are using microprocessors and microcontrollers. *EDN* is constantly uncovering companies that previous editions of the directory did not list. If you notice a company that we omitted, please let it and us know that you missed it and would like to see it in the next update of the directory.

The print version of this directory is but a small fraction of the entire directory, which stresses what is new over the last year for each company. Visiting the Web version at www.edn.com/microdirectory has taken on more importance as the company roster continues to expand the material of hundreds of pages well beyond the capacity of the print update. The print version lists the companies selling software-programmable processors and cores and provides an overview for each as well as identifies the latest developments over the previous year at each company.

This year's online version makes it easier to find the third-party-software-development companies by placing them in a companion directory that is cross-linked on the main pages of each listing. This directory aims to provide designers and system architects enough visibility into processor options to quickly narrow the list of candidate processors for each project. The expanded online section presents each processor, with detailed information and block diagrams. The directory uses a common taxonomy for describing and categorizing target applications that helps you to quickly find and compare competing processors for your projects. The Web material has more details on the common application taxonomy so that you can comment on it, and we can refine it as appropriate.

The "Where are they now?" **sidebar** on the Web helps you find companies that we no longer list, whether because they closed their doors, changed their focus (think National Semiconductor), another company acquired them, or they spun off into a different company. As always, the Web site duplicates and greatly expands upon the material you find in the print version.

IF THIS DIRECTORY HELPS YOU FIND OR CHOOSE A DEVICE OR CORE, PLEASE LET THE VENDOR KNOW HOW YOU FOUND ITS PART. HELP US CONTINUE TO IMPROVE THE DIRECTORY BY VISITING US AT WWW.EDN.COM/MICRODIRECTORY OR BY SENDING YOUR COMMENTS AND FEEDBACK TO MICRODIRECTORY@EDN.COM.

★ACTEL, WWW.ACTEL.COM

Actel offers low-power and mixed-signal FPGAs that support ARM and 8051 cores, including a license- and royalty-free, 32-bit, FPGA-optimized ARM Cortex-M1 processor. This year, the company introduced the ProASIC3L FPGAs, which feature 40 and 90% lower dynamic and static power, respectively, than the ProASIC3 FPGAs. Actel introduced its 15,000-gate, low-power Igloo AGL015 and ProASIC3 A3P015 FPGAs, available for 99 cents, and unveiled the Igloo PLUS family of FPGAs. On the tool side, Actel rolled out enhanced versions of its Libero IDE (integrated development environment) with new tools, such as power-driven layout, advanced power analysis, and battery-life estimation, to enable designers to identify and reduce sources of power consumption within their designs.

★ADVANCED MICRO DEVICES, WWW.AMD.COM

AMD's (Advanced Micro Devices') x86-based products span the consumer embedded-system market and serve enterprise-class servers and workstations, extending the x86 ISA (instruction-set architecture) across 32- and 64-bit PC, server, and workstation platforms. The company's x86 Geode processors bring target applications for the entertainment, business, education, and embedded-system markets. Opteron processors with Direct Connect Architecture and HyperTransport Technology enable the transition to 64-bit computing without sacrificing legacy x86 technology. Athlon 64 processors provide dual- and single-core computing for desktops that can run 32-bit applications while enabling 64-bit software applications. Turion 64 mobile technology enables thinner and lighter notebook PCs. The Mobile Sempron processor features range from lower power to full-sized mobile computing.

★ALTERA, WWW.ALTERA.COM

Altera's Nios II family of soft embedded processors features a general-purpose, 32-bit RISC CPU architecture in three configurations. The Nios II/f core emphasizes processing performance, the Nios II/e focuses on economy, and the standard Nios II/s core configuration balances performance and core size. The Nios II includes 32-bit, single-precision, IEEE 754-compatible, floating-point support and the Nios II C2H (c-to-hardware) compiler. Designers add Nios II processors to their systems using the SOPC (system-on-programmable-chip) Builder tool. The Nios II C2H-acceleration compiler enables developers to convert performance-critical C-language subroutines into hardware accelerators.

★ALTIUM, WWW.ALTIUM.COM

The Altium Designer development system combines board-level hardware, embedded software, and programmable hardware-development tools in a unified environment. It supports interactive FPGA-system development for device- and vendor-independent electronic-product development using soft, hybrid, and discrete processors. Altium Designer includes a number of royalty-free, 8- and 32-bit, FPGA-based soft processors, including Altium's FPGA-independent TSK3000RISC core. You can also use Altium Designer to target development for Nios II and MicroBlaze soft processors, the PowerPC within Xilinx's Virtex II Pro devices, and discrete ARM7 and PowerPC devices.

★ANALOG DEVICES, WWW.ANALOG.COM

Analog Devices' ADuC product family combines ARM7 or 8052 microcontroller cores with integrated precision converter, reference, and sensor peripherals to target automation, industrial, and automotive applications. The new ADuC706x family incorporates two 24-bit sigma-delta ADCs and analog peripherals with a 32-bit ARM7 core to target precision sensing applications. The company's Blackfin processor family combines signal-processing capabilities with control functions in a single 16/32-bit core. Target applications include audio and video consumer products, medical electronics, video surveillance, VOIP (voice over Internet Protocol), and industrial instrumentation and control.

★APPLIED MICRO CIRCUITS CORP, WWW.AMCC.COM

AMCC (Applied Micro Circuits Corp) offers embedded Power Architecture processors targeting control-plane, imaging, wireless-access, industrial-control, storage, and networking applications. The AMCC Power Architecture supports low-power operation; PCIe (peripheral-component-interconnect-express) and PCI-X (PCI extended) 2.0 I/O interfaces, interfacing to DRAM, such as DDR2 SDRAM; accelerated GbE (gigabit Ethernet); and security. An ecosystem of partners supplies operating systems, development tools, embedded software, board-level products, design services, and technical training.

The next-generation PowerPC 460GT and PowerPC 460GTx, based on the Power Architecture, target enterprise-class networking, storage, and wireless-infrastructure applications; high-performance, low-power, network-control applications; home gateways; and imaging/printing and NAS (network-attached-storage) applications. AMCC also announced the PowerPC 460SX storage processor for high-throughput RAID (redundant-array-of-inexpensive-disks) acceleration and interoperability with 6G SAS (6-Gbps serial-attached SCSI) and 8G FC (8-Gbps Fibre Channel).

AMCC announced complete hardware- and software-reference designs with Makalu for the wireless-access-point market and Arches for system innovators in the ATCA (Advanced Telecom Computing Architecture) AMC (advanced-mezzanine-card) market. Over the previous year, AMCC and Intrinsity joined forces to create a new Power Architecture processor core. Code-named Titan, the 32-bit semicustom core relies heavily on Intrinsity's Fast14 logic to reach clock speeds as high as 2 GHz in 90-nm bulk CMOS and consumes 2.5W. Titan is part of a dual-core "processor complex" that supports coherent multiprocessing.

★ARC INTERNATIONAL, WWW.ARC.COM

ARC International licenses consumer IP (intellectual property) in the form of multimedia subsystems and related technologies. Sonic Focus, an ARC International company, licenses audio-enhancement software. The new, fully programmable ARC Sound 210E subsystem targets high-quality audio for a low-power budget. ARC's new Energy Pro technology reduces SOC (system-on-chip) power consumption by as much as fourfold. ARC subsystems include a set of optimized and preintegrated audio, imaging, and video codecs, as well as development tools. The products target applications such as cell phones, portable media players, mobile TV handsets, and DVRs. The ARChitect configuration tool enables developers to explore and create an ARC subsystem or processor tailored to an application's requirements.

★ARM, WWW.ARM.COM

ARM licenses semiconductor IP (intellectual property), including processors, peripherals, interconnects, and physical libraries targeting mobile, automotive, consumer-entertainment, imaging, networking, storage, security, and wireless applications. The company's range of processors includes the ARM7, ARM9, ARM10, and ARM11 families and the Cortex family featuring Thumb-2 technology. ARM also offers the SecurCore processor family targeting secure applications, such as smart cards and SIMs (subscriber-identity modules), and the Mali family of graphics processors. ARM's supporting software includes TrustZone technology for data security and DRM (digital-rights management), Jazelle execution environment-acceleration software, IEM (Intelligent Energy Manager) technology, and RealView development tools.

The high-performance ARM Cortex-A9 MPCore multicore processor features energy-efficient, scalable performance. The ARM Cortex-A8 processor targets consumer products running multichannel video, audio, and gaming applications with a power consumption of less than 300 mW in a 65-nm technology. The midrange Cortex-R4 processor targets next-generation embedded products, including mobile phones, hard-disk drives, printers, and automotive controllers. Its microarchitecture can issue dual instructions. The ultracompact ARM Cortex-M3 processor targets cost-sensitive embedded-system applications, such as automotive-body systems, white goods, and networking devices. The ARM Cortex-M1 processor is the smallest ARM processor for implementation in FPGAs.

★ASIX ELECTRONICS, WWW.ASIX.COM.TW

Asix Electronics offers non-PCI (peripheral-component-interconnect)-Ethernet controllers, USB (Universal Serial Bus) 2.0-to-Ethernet NIC (network-interface-card) controllers, and network SOCs (systems on chips) targeting embedded-networking applications, such as home appliances, factory/building automation, industrial equipment, security systems, remote-control/monitoring/management, and streaming-media applications. Asix recently announced the availability of the single-chip AX11005BF, which comes in an 8×8-mm, 80-pin TFBGA package that integrates an 8-bit microcontroller with 512 kbytes of flash memory, TCP/IP (Transmission Control Protocol/Internet Protocol), and Fast Ethernet MAC (media-access-control) and PHY (physical) interfaces. Over the last year, Asix has focused on new processors that target wireless-networking applications. The single-chip AX220xx microcontroller with TCP/IP and 802.11 WLAN (wirelesss-local-area network) MAC/baseband includes a high-performance, dual-CPU architecture with 1 Mbyte of on-chip flash memory, a TCP/IP accelerator, an 802.11a/b/g-compatible WLAN MAC/baseband, Fast Ethernet MAC, and communication peripherals for applications that access wired or wireless LANs or the Internet.

★ATMEL, WWW.ATMEL.COM

Atmel's microcontrollers include the 8-bit AVR and 32-bit AVR32, ARM7, ARM9, and ARM11 cores. Three new ARM9-based processor families include the 400-MHz AT91SAM9920, which consumes 80 mW in active mode. The 200-MIPS flash AT91SAM9XE has boot ROM, a USB (Universal Serial Bus) host/device, Ethernet MAC (media-access control), a cryptographic engine, multiple serial interfaces, and DMA. The AT91SAM9RL64 supports real-time "smart" control panels with LCD and touchscreen controllers, a high-speed USB device, 24-channel DMA, a six-layer bus, and a 64-kbyte SRAM.

Atmel's less-than-100-nA picoPower microcontrollers include the 8-bit, AVR-based ATtiny48, the ATtiny88, the AVR Xmega family with true 1.6V operation, and the 32-bit ARM7-based AT91SAM7L. The new QProx touch-control and -sensing devices use patented charge-transfer technology to support capacitive-touch controls for automotive, industrial, appliance, and consumer-electronics applications. The new AVR Xmega families extend the 8-bit application range and bandwidth with 1.6V operation; a 32-MHz CPU; a DMA and event system; multilevel interrupts; AES (Advanced Encryption Standard)- and DES (Data Encryption Standard)-cryptography support; and a fast, 12-bit ADC and DAC.

All AVR microcontrollers share the same sin-

Analog Applications Journal

DESIGN BRIEF

Selecting Antennas for Low-Power Wireless Applications

By Audun Andersen
Field Application Engineer, Low-Power Wireless

Introduction

The antenna is a key component in an RF system and can have a major impact on performance. High performance, small size, and low cost are common requirements for many RF applications. To meet these requirements, it is important to implement a proper antenna and to characterize its performance. This article describes typical antenna types and covers important parameters to consider when choosing an antenna.

Antenna Types

Antenna size, cost, and performance are the most important factors to consider when choosing an antenna. The three most common antenna types for short-range devices are PCB antennas, chip antennas, and whip antennas. Their pros and cons are shown in Table 1.

Antenna Parameters

Some of the most important things to consider when choosing an antenna are: the radiation pattern, antenna efficiency, and antenna bandwidth.

Radiation Pattern and Gain

Figure 1 shows how the radiation pattern from a PCB antenna varies in different directions in the plane of the PCB. Several parameters are important to know when interpreting such a plot. Some of these parameters are stated in Figure 1.

In addition to the plot information, it is important to relate the radiation pattern to the positioning of the antenna. Radiation pattern is typically measured in three orthogonal planes, XY, XZ and YZ. It is possible to perform full 3D pattern measurements, but it is usually not done because it is time consuming and requires expensive equipment.

Table 1. Pros and Cons for Antenna Types

Types	Pros	Cons
PCB Antenna	• Low cost • Good performance is possible • Small size is possible at high frequencies	• Difficult to design small and efficient antennas • Potentially large size at low frequencies
Chip Antenna	• Small size	• Medium performance • Medium cost
Whip Antenna	• Good performance	• High cost • Difficult to fit in many applications

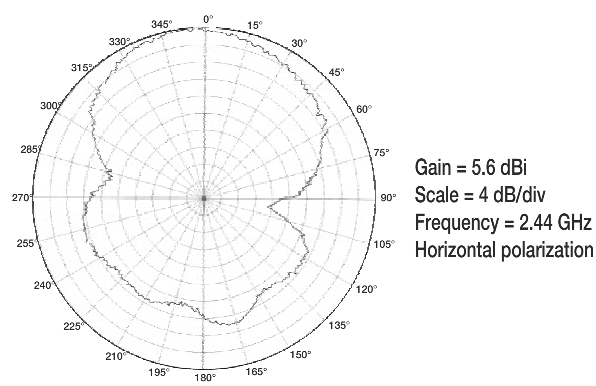

Figure 1. Radiation pattern.

The gain, or reference level, usually refers to an isotropic radiating antenna, which is an ideal antenna with uniform radiation in all directions. When an isotropic antenna is used as a reference, the gain is given in dBi or specified as the effective isotropic radiated power (EIRP). The outer circle in Figure 1 corresponds to 5.6 dBi and the 4-dB/div label means that for each progressively smaller circle, the emission level is reduced by 4 dB. Compared to an isotropic antenna, the PCB antenna will have a 5.6-dB higher level of radiation in the 0° direction.

As shown by Equation 1, antenna gain, G, is defined as the ratio of maximum-to-average radiation intensity multiplied by the efficiency of the antenna.

$$G = e \times D = \frac{P_{rad}}{P_{in}} \times D = \frac{P_{rad}}{P_{in}} \times \frac{U_{max}}{U_{avg}}, \quad (1)$$

where U_{max} is the maximum radiation intensity, U_{avg} is the average intensity, and the ratio of these two values is known as directivity, D. Ohmic losses in the antenna element and reflections at the antenna feed point determine the efficiency, e, which is simply the radiated power, P_{rad}, divided by the input power, P_{in}. High gain does not automatically mean that the antenna has good performance. Typically, mobile systems require an omnidirectional radiation pattern so the performance will be about the same for any antenna orientation.

To accurately measure an antenna radiation pattern, it is important to measure only the direct wave from the device under test and avoid reflecting waves that could affect the result. To minimize picking up reflected energy, measurements are often performed in an anechoic chamber or at an antenna range. Another requirement is that the measured signal must be a plane wave in the far field of the antenna. The far field distance, R_f, is determined by the wavelength, λ, and the largest antenna dimension, DIM, as shown by Equation 2. Since the size of anechoic chambers is limited, it is common to test large, low-frequency antennas in outdoor ranges.

$$R_f = \frac{2 \times DIM^2}{\lambda} \quad (2)$$

Bandwidth and Impedance Matching

A common method to determine antenna bandwidth is to measure the radiated power while stepping a carrier across the frequency band of interest. Figure 2 shows the first method which is measurement of radiated power from a 2.4-GHz antenna that has approximately 2-dB variation in output power across the 2.4-GHz frequency band and has maximum radiation near the center of this band. This measurement was done by stepping a continuous-wave signal from 2.3 GHz to 2.8 GHz. Such measurements

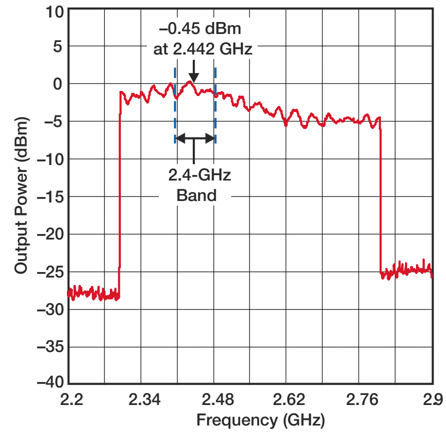

Figure 2. Bandwidth of a 2.4-GHz antenna.

should be performed in an anechoic chamber to obtain a correct absolute level. However, this measurement can be very useful even if an anechoic chamber is not available.

A second method to determine bandwidth is measuring the reflection at the antenna feed point with a network analyzer. See Reference 1 for details.

Size, Cost and Performance

The ideal antenna is infinitely small, has zero cost and has excellent performance. In real life, however, a compromise between parameters is necessary. For example, decreasing the operating frequency by a factor of two can double the RF range. Thus, one of the reasons to operate at a lower frequency is often to achieve longer range. The down side is that most antennas need to be larger at lower frequencies to achieve good performance. In some cases where the board space is limited, a small, efficient high-frequency antenna may provide equal or greater range performance than a small, inefficient low-frequency antenna. A chip antenna is a good alternative when seeking a small antenna solution. This is particulary true with frequencies below 1 GHz because the chip antenna will allow a much smaller solution than the traditional PCB antenna. The main drawbacks with chip antennas are the increased cost and typically narrow-band performance.

Antenna Reference Designs

Texas Instruments offers a wide range of RF products designed to operate in license-free frequency bands. See Reference 2 for more information.

References

Please see Reference 1 for the complete version of this article, which includes more information about choosing antenna types, antenna polarization, and another method to characterize antenna bandwidth.

1. View the complete article at http://www-s.ti.com/sc/techlit/slyt296
2. www.ti.com/lpw

gle-cycle CPU and target both the 8- and 16-bit-system markets with function-, pinout-, and layout-compatible AVR families. The company offers unified cross-platform tools for AVR through AVR32 designs that include the ATSTK600 AVR starter kit and the AVRone! debugger/programmer platform with JTAG, debugWire, PDI, and Nexus support. The ZigBee-certified, ready-to-deploy RZ Raven platform targets 2.5-GHz wireless designs.

★NEW AUSTRIAMICROSYSTEMS AG, WWW.AUSTRIAMICROSYSTEMS.COM

Austriamicrosystems offers high-performance analog ICs with a focus on power management, sensors and sensor interfaces, and portable audio. The company's 200-MIPS, ARM9TDMI-based AS3525/27 integrated-audio-processor system combines strong calculating power, high-performance-audio features, and system-power-management options for battery-powered devices. The AS353x family integrates hardware accelerators for MP3, WMA (Windows Media Audio), and AAC (Advanced Audio Coding) for audio; WMV9 (Windows Media Video Version 9) Main Profile and Sorenson Spark for video; and high-performance postprocessing for enhanced GUIs (graphical user interfaces).

★NEW BEYOND SEMICONDUCTOR, WWW.BEYONDSEMI.COM

Beyond Semiconductor licenses two families of 32-bit processor cores available as Verilog RTL source or ChipX hard macros. All processors come with industry-standard software-development tools and OS support, including Linux and eCos. The modern, superscalar Beyond BA14 processor features dual-issue, out-of-order execution. With powerful DSP instructions and an optional double-precision floating-point unit, it targets applications with demanding performance requirements. The Beyond BA22 processor can replace obsolete 8- and 16-bit processors. Implementing four-way cache and TLBs (translation-look-aside buffers) enables the Beyond BA22 to run modern Linux-multimedia applications.

★BROADCOM, WWW.BROADCOM.COM

Broadcom provides a family of high-performance, low-power, integrated processors targeting data-networking and communications applications, as well as security, storage, 3G-wireless infrastructure, and high-density computing. The Broadcom broadband CMP (chip-multiprocessing) systems integrate as many as four 64-bit MIPS processor cores onto a single die.

★CAMBRIDGE CONSULTANTS, WWW.CAMBRIDGECONSULTANTS.COM

Cambridge Consultants' XAP3, XAP4, and XAP5 family of RISC-processor soft cores targets low-cost ASIC products, such as medical technology, industrial and consumer products, automotive systems, transportation, and wireless communications. The company's mixed-signal and wireless SOC (system-on-chip) systems support wireless standards, such as Bluetooth, ZigBee, and UWB (ultrawideband). XAP processors feature protected operating-system modes with register sets for user, supervisor, and interrupt code to provide secure operation when applications misbehave. Designers can implement the 16-bit XAP4 using as few as 12,000 gates. The 18,000-gate, 16-bit XAP5 processor has a 24-bit address bus that can run programs as large as 16 Mbytes. The 32-bit XAP3 processor has 30,000 gates.

★CAST, WWW.CAST-INC.COM

Cast offers IP (intellectual-property) cores for general-purpose 8-, 16-, and 32-bit processors. A configurable 8051 core executes instructions with one clock per cycle. Additional cores include 8-bit Z80 and 16-bit 68000- and 80186EB-compatible devices. They require as few as 7000 gates, perform at 0.6 Dhrystone MIPS/MHz, and use as little as 18 μW/MHz of power. A coprocessor architecture enables performance improvement for specific applications, and an ASP-DSP coprocessor is available.

★CAVIUM NETWORKS, WWW.CAVIUM.COM

Cavium Networks offers single-core and multicore MIPS64-based processors targeting networking, wireless, storage, and control-plane applications in the broadband consumer, SOHO (small-office/home-office), SME (small-and-midsized-enterprise), enterprise, data-center, telecom, ATCA (Advanced Telecom Computing Architecture), AMC (advanced-mezzanine-card), 3G/4G, and service-provider markets. The Octeon MIPS64 processors integrate one to 16 MIPS64 cores with high-performance networking, multicore acceleration, memory controllers, and hardware-acceleration coprocessors for TCP (Transmission Control Protocol), compression, decompression, regular expression, and security. The Nitrox Security processors accelerate IPsec (Internet Protocol Security), SSL (Secure Sockets Layer), and WLAN (wireless-local-area-network) and encryption algorithms, such as 3DES (Triple Data Encryption Standard), AES (Advanced Encryption Standard), RSA (Rivest/Shamir/Adleman), DH (Diffie-Hellman), Kasumi for 3 and 4G applications, and AES-XTS (Xor-Encrypt-Xor-based Tweaked CodeBook) for disk encryption.

★CIRRUS LOGIC, WWW.CIRRUS.COM

Cirrus Logic supplies high-precision analog- and mixed-signal and embedded processors for the audio and industrial markets. In the general-purpose processor segment, Cirrus Logic offers highly integrated ARM9- and ARM7-based embedded processors targeting industrial and networked consumer applications. Cirrus Logic's NineSeries of ARM9-based products includes the EP9301, EP9302, EP9307, EP9312, and flagship EP9315. The entry-level EP9301 integrates Ethernet and two USB (Universal Serial Bus) 2.0 host ports, and the EP9302 adds MaverickCrunch and MaverickKey to go along with increased processing power and memory. The EP9307 adds a graphics accelerator, touchscreen and keypad support, and three USB ports. The EP9312 supports high-quality audio and an integrated development environment. The flagship EP9315 adds support for the PCMCIA (Personal Computer Memory Card International Association) interface in a single device.

★CRADLE TECHNOLOGIES, WWW.CRADLE.COM

Cradle's CT3600 family of scalable MDSP (multicore-digital-signal-processing) processors integrates multiple general-purpose processors with multiple DSPs for control code and computationally intensive media-processing algorithms. Targeting media-processing applications, particularly those involving complex, intelligent-video applications, the CT3600 family comprises two products containing eight to 16 DSP processors on a single chip. The largest version, with 16 DSPs and eight general-purpose processors, operates at 350 MHz, and supports 16 channels of CIF (common-intermediate-format)-resolution Simple Profile MPEG-4 encoding.

★CYAN TECHNOLOGY, WWW.CYANTECHNOLOGY.COM

Cyan Technology's low-power, 16-bit, embedded-communications, flash-based eCOG1k microcontroller implements a 25-MHz RISC Harvard architecture that includes internal flash memory, RAM, and cache. The external-memory interface supports addressability of 32 Mbytes of external memory. Additional features include a smart-card interface, a 12-bit ADC, a temperature sensor, and a proprietary-port configuration device.

★CYBERNETIC MICRO SYSTEMS, WWW.CONTROLCHIPS.COM

Cybernetic Micro Systems produces ASICs to interface to peripherals that would be difficult to control from a general-purpose computer. The 100-pin, 8-bit P-51 microcontroller either sits between the host computer and the peripheral device or becomes the peripheral device. With a dual-port RAM interface on the host side in a PC104/ISA (industry-standard-architecture) format, the P-51 looks like memory to the host, but it has the intelligence and capability of an 8051.

★CYPRESS MICROSYSTEMS, WWW.CYPRESSMICRO.COM

Cypress' mixed-signal PSOC (programmable system on chip) features configurable digital and analog peripherals, an 8-bit microcontroller, and three types of embedded memory. Target applications include automotive, communications, computers and peripherals, consumer, industrial, and mobile/wireless.

This year, Cypress introduced the PSOC-based CapSense Express capacitive touch-sensing technology for button and slider replacement, which enables designers to implement as many as 10 buttons, sliders, or both in minutes with no coding. PSOC's CapSense touch-sensing function offers single-chip integration of multiple buttons, sliders, touchpads, and proximity detection. The PSOC-based TrueTouch single-chip touchscreen can interpret as many as 10 inputs from all areas of the screen simultaneously. TrueTouch supports projected capacitive touchscreens.

The new CY8C23x33 PSoC features an enhanced ADC for fast analog sampling and expanded flash-memory capacity for complex algorithm processing, targeting motor control and other applications with rich feature and software content. To improve design support for PSOC products, Cypress released PSOC Designer 5.0, the industry's only IDE (integrated design environment) that includes both code-free and high-level-language-programming modes in one package.

★DIGI INTERNATIONAL, WWW.DIGI.COM

Digi International offers net-centric NET+ARM processors based on ARM7 and ARM9 cores. The NS9215 and NS921 networking processors with ARM926EJ-S cores operate at 75 and 150 MHz; both chips feature 10/100-Mbps Ethernet. The NS9360, NS9750, and NS9775 employ the ARM926EJ-S core. The NS9360 operates at 177 MHz and integrates 10/100-Mbps Ethernet, USB (Universal Serial Bus), an LCD, IEEE 1284, and serial I/O. The NS9750 operates at 200 MHz and includes all of the NS9360 features, plus PCI (peripheral-component-interconnect) support. The NS9775 color-laser-printer processor operates at 200 MHz and integrates 10/100-Mbps Ethernet, USB, and PCI to improve the cost performance of color-laser printers. Digi based the NS7520 on the ARM7TDMI core. It operates at 55 MHz and integrates 10/100-Mbps Ethernet, serial I/O, and a general-purpose interface. Digi supports development for the 32-bit NET+ARM microprocessor with its royalty-free NET+OS advanced networking software, development tools, and real-time operating system. Support for Linux and Microsoft Windows Embedded CE 6.0 is also available.

★DIGITAL CORE DESIGN, WWW.DCD.PL

DCD (Digital Core Design) provides VHDL and Verilog synthesizable, ISO 9001:2000-certified IP (intellectual-property) cores of 8-, 16-, and 32-bit processors and bus interfaces, as well as fixed- and floating-point arithmetic coprocessors. DCD's DP8051XP/DP80390XP soft core is 100% binary-compatible with the 8051 microcontroller. Its SXDM (synchronous-external-data-memory) interface enables fast access to external data memory. DP8051XP/DP80390XP dual data pointers with automatic-increment, -decrement, and -switching capabilities significantly speed memory operations. DCD's microcontrollers implement fast 16- and 32-bit integer operations and single- and double-precision floating-point operations.

★NEW E2V, WWW.E2V.COM

E2V purchased its Grenoble, France, facility from Atmel in 2006 and has introduced products to its suite of high-reliability microprocessors and MRAMs (magnetic-random-access memories) in partnership with Freescale Semiconductor, broadband-data converters, ASICs, and ISM (industrial/scientific/medical) transceivers targeting defense, space, avionics, telecom, industrial, medical, and automotive applications. E2V's microprocessor products range from the 68K family to the new-generation PowerPC devices and support peripherals in partnership with Tundra Semiconductor. In addition to test and service facilities, the company offers long-term availability on the complete family of products. New products over the last year include a multichannel, 8-bit ADC operating beyond 1G sample/sec; the EV2A16A MRAM, an extended-reliability version of the MR2A16A from Freescale Semiconductor; and the CAPRI2.0 mixed-signal-ASIC-development kit.

★EM MICROELECTRONIC, WWW.EMMICROELECTRONIC.COM

EM Microelectronic offers ultralow-power, low-voltage, digital-, analog-, and mixed-signal ICs targeting battery-operated and field-powered devices in consumer, automotive, and industrial applications. EM Microelectronic's 4- and 8-bit microcontrollers target battery-operated devices, which often have low-standby-power requirements and perform periodic or on-demand actions. Such devices include fire alarms, medical-monitoring devices, sports-activity monitors, radio-controlled clocks, intelligent sensors, data loggers, metering devices, intelligent terminals, card readers, measurement devices, and scales.

★FREESCALE SEMICONDUCTOR, WWW.FREESCALE.COM

Freescale Semiconductor offers processors, sensors, RF components, analog/power-management technology, and supporting software for automotive, consumer, industrial, networking, and wireless applications. Freescale bases its PowerQUICC (quad-integrated-communications-controller) processors on Power Architecture cores. PowerQUICC processors provide data- and control-plane processing for wireless and wire-line infrastructure, industrial control, enterprise networking, home and SOHO (small-office/home-office) networking, and pervasive computing. Freescale introduced the QorIQ line of multicore embedded processors, the next generation of PowerQUICC processors, targeting developers migrating to multicore designs.

This year, the company's Controller Continuum road map added Flexis-series devices for consumer and industrial markets, including a new Flexis family for large-appliance applications. Flexis pin-for-pin-compatible 8- and 32-bit microcontrollers come with a set of on-chip peripherals and development tools. The company expanded its ColdFire portfolio with new processors targeting touchscreen-LCD applications. The automotive-microcontroller line adds controllers employing S08, S12X, and Power Architecture cores, including 32-bit devices that Freescale co-developed with STMicroelectronics.

Freescale bases its i.MX application processors on ARM core technology. They target embedded, general-purpose-system and multimedia applications for homes, handheld devices, and cars. The processors employ Smart Speed technology to balance high performance with battery life. The new i.MX37 multimedia application processor targets the PMP (portable-media-player), mobile-Internet, and portable-GPS (global-positioning-system)-navigation markets. Based on the ARM1176JZF-S core, the device targets price-sensitive consumer-application markets with advanced user-interface features. The i.MX31 multimedia application processors, which the company based on the ARM1136JF-S core, include video and 3-D-graphics accelerators, a vector floating-point unit, and numerous connectivity options. Reference designs are available for mobile and videoconferencing phones, PMPs, intelligent remote controls, and portable-GPS applications.

★FUJITSU MICROELECTRONICS AMERICA, WWW.FMA.FUJITSU.COM

Fujitsu's 8-, 16-, and 32-bit microcontrollers include general-purpose and application-specific versions; most of the microcontrollers include onboard-flash, ROM, ADC, DAC, CAN (controller-area-network), USB, and LCD controllers to target automotive, communications, computer-peripheral, industrial, and consumer applications. Software- and hardware-development tools support these microcontrollers. The F2MC (Fujitsu flexible-microcontroller) line includes the 8-bit F2MC-8L and F2MC-8FX series and the 16-bit F2MC-16L/16LX/16F series. The FR (Fujitsu RISC) series has a stepper motor and LCD controllers.

★GAINSPAN, WWW.GAINSPAN.COM

GainSpan, a Wi-Fi (wireless-fidelity) semiconductor and software provider, targets applications such as temperature monitoring for energy management, condition monitoring of industrial equipment, and street-light monitoring for metropolitan areas that require Wi-Fi capability and five to 10 years of battery life. The GainSpan GS1010 Wi-Fi SOC (system on chip) integrates an 802.11b/g

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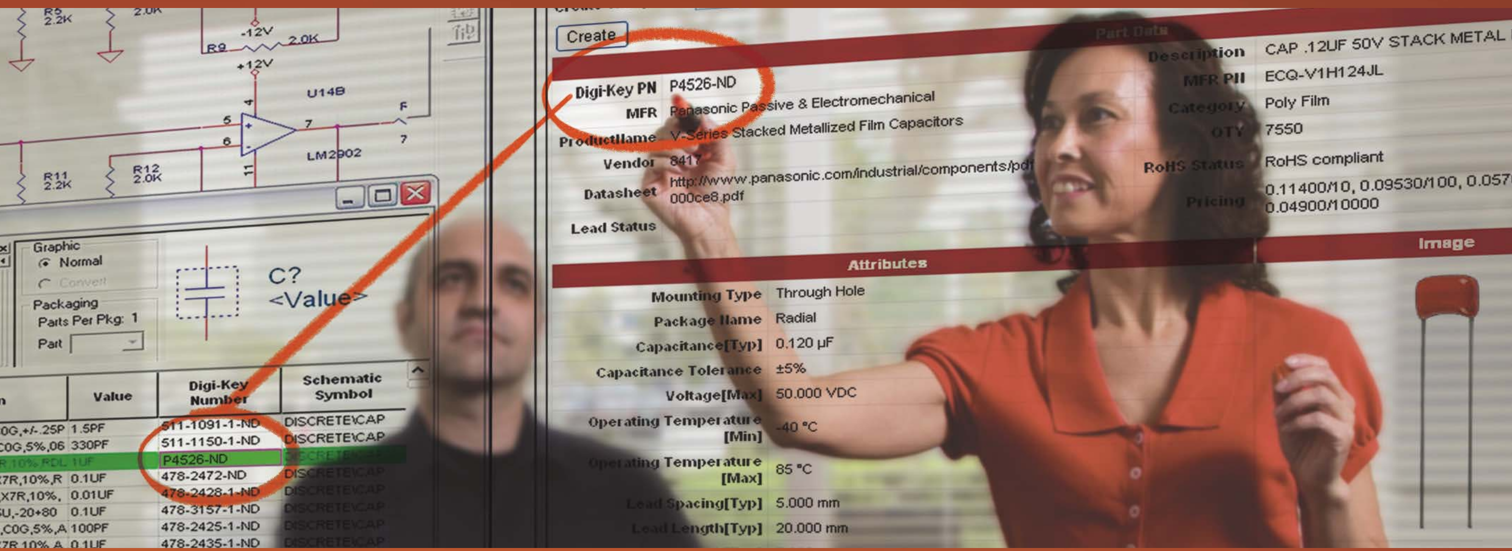

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radio, an ARM7 microcontroller, and a power-management unit. The GMS (GainSpan-management-system) software manages Wi-Fi devices that are asleep as much as possible to conserve energy. GMS resides in the network as an "always-on" intelligent interface.

★HYPERSTONE, WWW.HYPERSTONE.COM

Hyperstone offers the general-purpose E1 processors, the HyNet networking processors, and the NAND-flash controllers that the company based on a unified RISC/DSP architecture. This year, Hyperstone introduced the S7(B) SD/MMC (secure digital/multimedia card) and the F4 CF/PATA (CompactFlash/parallel-advanced-technology-attachment) NAND-flash-memory controllers. You can use the S7(B) SD 2.0/MMC 4.3 controller to produce high-performance SD and MMCs. The CFA3.0/ATA6F4 controller targets uses in high-performance CF cards and SSDs (solid-state disks). The S7(B) and F4 controllers support MLC (multilevel-cell) and SLC (single-level-cell) flash from all NAND-flash vendors. Manufacturing tools for the S7(B) and F4 NAND-flash-memory controllers include reference designs, development utilities, and operating firmware that implements Hyperstone's patented flash-management techniques.

★IBM, WWW.IBM.COM

IBM Global Engineering Solutions offers embedded-microprocessor cores and microprocessors employing IBM Power Architecture technology. IBM's offerings include the 32-bit PowerPC 4xx family of embedded cores, along with 32- and 64-bit power- and performance-optimized microprocessors. IBM's PowerPC 405, 440, and 460 families of embedded cores offer scalable performance for custom-SOC (system-on-chip) integration. The cores are available in both fab-optimized and fully synthesizable versions.

IBM's PowerPC 750 family of 32-bit microprocessors targets cost- and power-sensitive embedded-system applications. The 750CL is available at speeds as high as 1 GHz. The PowerPC 970 family of microprocessors offers a 64-bit architecture with native 32-bit application compatibility. Targeting computationally and bandwidth-intensive workloads, IBM's 970 family includes both single- and dual-core, VMX-enabled offerings.

★IMEC, WWW.IMEC.BE

IMEC's (Interuniversity Microelectronic Centre's) flexible ADRES (architecture for dynamically reconfigurable embedded system) consists of a tightly coupled VLIW (very-long-instruction-word) processor and a coarse-grained reconfigurable array. The architecture template consists of computational, storage, and routing resources. The routing resources connect the computational and storage resources in a topology to form the ADRES array. Data accesses to the memory of the unified architecture take place through load/store operations. A script-based technique allows designers to generate instances by specifying different values for the communication topology, supported operation set, resource allocation, and timing of the target architecture.

★IMSYS TECHNOLOGIES, WWW.IMSYSTECH.COM

Imsys develops reconfigurable-processor platforms that accept programs written in Java, C/C++, assembler, and microcode. The company offers Internet-enabled reference modules that Imsys ships as ready-to-go subsystems. The integrated hardware and software platform targets wired and wireless communications, graphics-display technologies, and image processing in telecom, automotive, industrial-automation, and consumer electronics.

★INFINEON TECHNOLOGIES AG, WWW.INFINEON.COM

Infineon Technologies AG semiconductor's 8-, 16-, and 32-bit industrial microcontrollers incorporate peripheral sets that target control algorithms for improved motor-drive performance with reduced external hardware and low software overhead. This year, Infineon expanded its 8-bit line of products by adding the XC878 and XC864 families, as well as a variety of development kits that allow designers to exploit the Vector Computer and other XC800 family functions for three-phase-motor-drive applications using FOC (field-oriented control). Infineon also extended its automotive portfolio with 16- and 32-bit microcontroller families. The 16-bit family provides cost-effective electronic-engine control in motorcycles, and the 32-bit family allows automobile-engine and transmission management for improved fuel efficiency and emission reduction.

★NEW INNOVASIC SEMICONDUCTOR, WWW.INNOVASIC.COM

Innovasic Semiconductor supplies extended-life microcontrollers for industrial applications. The fido1100 32-bit communications controller targets real-time Ethernet applications with RTOS-like features, including single-cycle task switching, scheduling, and programmable peripherals, embedded in silicon. This year, Innovasic introduced a real-time Ethernet solution for the fido1100 that includes a development module, which is available as a reference design or a product. A TCP/IP (Transmission Control Protocol/Internet Protocol) stack and libraries now support the device, and Ethernet/IP, Profinet, and QOS (quality-of-service) support will be available soon. Innovasic released Version 1.4 of the software-development kit with an application framework that, together with the silicon-RTOS features, enhances or even eliminates the need for an RTOS.

Innovasic supplies 16-bit 186 microcontrollers for new and legacy applications. This year, Innovasic released the 16-bit IA186EB and the IA186XLt 186 microcontrollers, which are fully compatible with their respective Intel devices.

★INTEGRATED DEVICE TECHNOLOGY, WWW.IDT.COM

The IDT Interprise family of integrated communications processors delivers data processing at line-rate speed. IDT based the processor cores on the 32-bit MIPS ISA (instruction-set architecture). Interprise processors target SOHO (small-office/home-office) routers, Ethernet switches, WAPs (wireless-access points), and VPN (virtual-private-network) equipment.

★INTEL, WWW.INTEL.COM

The 45-nm quad-core Intel Xeon processor 5400 series and dual-core Intel Xeon processor 5200 series are the first Intel Xeon processors that the company produced on 45-nm technology. They support an extended life cycle and employ a hafnium-based, high-k-metal-gate formula. This 45-nm process technology reduces power consumption, increases switching speed, and significantly increases transistor density over the previous 65-nm technology. The E5440 delivers a 22% performance gain within the same thermal profile over the previous-generation E5345, making the E5440 more suitable for computationally intensive embedded-system, storage, and communications applications.

★INTELLASYS, WWW.INTELLASYS.NET

IntellaSys based its multicore chips on the proprietary SEA (scalable-embedded-array) platform, which uses a dual-stack, synchronous, scalable architecture. The SEAforth-24 family packs a 634-processor array of 18-bit processors, each of which can operate at 1 BOPS (billion operations per second). Designers can dedicate any of the 24 cores individually or in groups to perform tasks. Because each core has its own ROM and RAM, there is no need to use external memory for the bulk of processing and data accesses. The SEAforth-24 directly drives an antenna, eliminating the need for external data converters.

★IPFLEX, WWW.IPFLEX.COM/EN

IPFlex offers dynamically reconfigurable processors and design-tool platforms targeting industrial-image-processing, network-security, and scientific-computing applications. The DAPDNA (digital-application-processor/distributed-network-architecture) series of processors incorporates a RISC processor as a controller and a heterogeneous matrix of 300 to 1000 16- to 32-bit processing elements that the system can reconfigure in a single clock cycle. The DAPDNA-2 and DAPDNA-IMS processors target image-inspection-system, network-security, and multifunction-printer applications.

★KAWASAKI MICROELECTRONICS (K-MICRO), WWW.K-MICRO.US

K-Micro's ASIC technologies and design support target the consumer-electronics, computer, office-automation, networking, and storage markets. K-Micro's computing subsystem includes a MIPS32 24Kf processor, the Sonics SiliconBackplane and Sonics3220 Smart interconnects, the SafeNet SafeXcel security engine, an off-chip OCP (Open Core Protocol) interface, on-chip SRAM, a flash-memory controller, a DMA interface, an interrupt controller, and a timer. To create an SOC (system on chip), designers add their proprietary logic to the computing subsystem. Single- and dual-core processors are available.

★LATTICE SEMICONDUCTOR, WWW.LATTICESEMI.COM

The 32-bit, open-source LatticeMico32 soft-microprocessor core combines a 32-bit-wide instruction set with 32 general-purpose registers. The flexible reference design suits a variety of applications. The architecture is configurable with a RISC-like instruction set. Lattice based the device on the Wishbone bus of OpenCores, and it has independent instruction paths and datapaths. Peripherals include GPIO (general-purpose-input/output), SPI (serial-peripheral-interconnect), I^2C (inter-integrated-circuit), trispeed-Ethernet-MAC (media-access-controller), DDR1, DDR2, and DMA controllers. OS support includes Micrium's µC/OS-II RTOS; the µITRON/JSP open-source RTOS, which Toppers developed in Japan; and µClinux.

You can download the LatticeMico32 license agreement from the Lattice Web site. The license preserves the open nature of the core by permitting use alongside proprietary designs and allows hardware implementation and distribution without the need for a subsequent license agreement. The MSB (Mico-system-builder) module of the LatticeMico32 system generates the core design, which is in Verilog. The MSB tool supports the design of microprocessor-based systems. The LatticeMico32 system comes with GNU-based C/C++ software-development tools and the GDB (GNU debugger).

Lattice also provides an open-source 8-bit microcontroller, the LatticeMico8, as well as microcontrollers, including the 8051, 68xx series, PIC, and 6502, through its partners: Cast, Digital Core Design, and Western Design Center.

★LUMINARY MICRO, WWW.LUMINARYMICRO.COM

Luminary Micro designs, markets, and sells more than 80 ARM Cortex-M3-based microcontrollers. The Cortex-M3 processors provide 32-bit performance and integration for a price similar to that of 8- and 16-bit devices. The Stellaris family targets applications requiring control processing and connectivity, such as motion control, medical instrumentation, HVAC (heating/ventilation/air conditioning) and building control, factory automation, transportation, remote monitoring, electronic point-of-sales machines, network appliances, and gaming equipment.

★MAXIM INTEGRATED PRODUCTS, WWW.MAXIM-IC.COM

Maxim Integrated Products offers the networked, secure, mixed-signal, and 8051-drop-in families of microcontrollers. The company has expanded the MAXQ mixed-signal line of parts to include more LCDs, USB (Universal Serial Bus) interfaces, and voltage regulators. Maxim also introduced a family of electricity-metering parts that integrates the major components necessary for electricity meters. The product line includes both analog-front-end-interface devices and specialized microcontrollers that automatically perform necessary electricity-metering functions, such as measuring active, reactive, forward, and reverse power; line frequency; power factor; and phase angle. Some devices within the family can generate an interrupt on exceptional conditions, thus warning the system of possible problems.

The company has expanded its secure-microcontroller family with cryptographic peripherals. The secure microcontrollers target applications that require protective measures against theft of proprietary or secret information. The devices employ encryption and physical-protection techniques that support point-of-sale terminals, automated-teller machines, banking, and gaming equipment.

Maxim's network microcontrollers include an optional, complete TCP/IP (Transmission Control Protocol/Internet Protocol) network stack in ROM, an Ethernet MAC (media-access controller), a CAN (controller-area network), and parallel and serial ports. The devices use a four-clock-per-machine-cycle 8051 core that operates as fast as 75 MHz with an extended 22-bit addressing range and 16 Mbytes of direct addressing.

★MICROCHIP TECHNOLOGY, WWW.MICROCHIP.COM

Microchip Technology's family of PIC microcontrollers and dsPIC DSCs (digital-signal controllers) spans more than 500 8-, 16-, and 32-bit devices. The unified and free MPLab IDE (integrated development environment), a broad selection of powerful but inexpensive starter kits and development platforms, and an extensive library of free software and middleware support the devices. The portfolio spans from low-cost, six-pin, 8-bit microcontrollers through the new high-performance, cost-effective, 64- and 100-pin, 80-MHz, 32-bit PIC32 family.

This year, Microchip introduced the 32-bit PIC32 family with 80-MHz performance and as much as 512 kbytes of flash memory, which maintain the unified Microchip-development experience. The company introduced more than 50 16-bit PIC24 microcontrollers with expanded peripherals and memory. The company released

THE RIGHT

26 new dsPIC DSCs, delivering peripherals and performance for motor-control, power-supply, and general-purpose-embedded-system applications. The company expanded the capabilities of the 8-bit PIC microcontroller family with enhanced performance, improved power management and consumption, and broader operating voltages. Across the full portfolio, Microchip introduced 37 products with a selection of USB (Universal Serial Bus) device, host, dual-role, and OTG (On-The-Go) capabilities. Microchip also released development tools, platforms, and starter kits.

★MIPS TECHNOLOGIES, WWW.MIPS.COM

MIPS Technologies offers processor and analog IP (intellectual property), as well as software tools for the embedded-system market. MIPS' cores range from the low-power MIPS32 M4K core to extremely high-performance, single-threaded and multithreaded cores, such as the MIPS32 24K and MIPS32 1004K. The company recently introduced the coherent-processing, multithreaded, multiprocessor, licensable-IP MIPS32 1004K core. In the past year, MIPS also announced the PIC32-microcontroller family, representing the company's entry into the 32-bit-microcontroller market.

MIPS cores and architectures have the support of an ecosystem of standard tools, IP, hardware, software, and services, including the new MIPS Navigator ICS (integrated-component suite), which enables embedded developers to code, debug, and analyze Linux systems on MIPS-based embedded systems.

★NEC ELECTRONICS AMERICA, WWW.AM.NECEL.COM

NEC Electronics America offers low-power, all-flash microcontrollers for multipurpose and application-specific devices, including consumer, mobile, health-care, industrial, and automotive applications. The company has expanded its microcontroller support for multipurpose, consumer, mobile, LED-lighting, health-care, and industrial applications, as well as automotive-vision, connectivity, and infotainment systems.

The company's 32-bit V850 series microcontrollers feature low-voltage operation, DSP functions, and on-chip peripherals. The new V850ES/Jx3-H and V850ES/Jx3-U microcontrollers suit use in industrial- and consumer-electronics systems that require USB (Universal Serial Bus) connectivity. The V850ES/Jx3-L microcontrollers target battery-powered portable industrial and health-care devices. The V850ES/PH03 microcontroller, with embedded FlexRay technology, and the V850ES/Fx3-L microcontrollers target automotive chassis, inverter-control, body, and safety applications.

The new 78K0R/Kx3-L and 78K0R/Ix3 microcontrollers expand the company's 16-bit support for portable consumer, inverter-control, industrial, and health-care applications, with longer battery life and smaller devices. NEC Electronics America's 8-bit 78K0 and 78K0S microcontrollers target consumer and health-care devices; HVAC (heating/ventilation/air-conditioning); motor control; industrial controllers; and automotive-body, dashboard, and safety systems. A new high-current-drive/LED microcontroller also delivers intelligent power-management control for LED-lighting applications.

★NXP, WWW.STANDARDICS.NXP.COM/MICROCONTROLLERS

NXP offers a portfolio of more than 100 ARM7-, ARM9-, and 80C51-based microcontrollers. NXP's LPC3000 and LPC2000 ARM-based families include integrated peripherals, such as Ethernet, device and host USB OTG (On-The-Go), and CAN (controller-area-network), as well as many serial-communications peripherals. The LH7 and LH7A series devices, formerly from Sharp Microelectronics, feature high-performance integrated LCD controllers and available system-level systems.

★OKI SEMICONDUCTOR, WWW.OKISEMI.COM/US

Oki's Advantage Microcontroller family comprises ARM-core-based products ranging from the ML671000 with a built-in USB controller to the high-performance, 120-MHz, ARM946E-based 6200 series with instruction and data caches. Oki's 4060, 4050, 675K, and 674K series ARM7 Advantage microcontrollers offer variations in frequencies, memory sizes, caches, features, and packages.

★PA SEMI, WWW.PASEMI.COM

PA Semi offers high-performance, low-power 64-bit Power Architecture processors with highly integrated peripheral functions. The PA6T-1682M PWRficient processor implements a coherent, ordered-crossbar interconnect, two 2-GHz Power Architecture processor cores, 2 Mbytes of L2 cache, two DDR2-memory controllers, multichannel DMA, and hardware-acceleration engines. The PA6T-1682M targets networking, telecom, storage, single-board-computer, industrial, and military-aerospace applications.

★PMC-SIERRA, WWW.PMC-SIERRA.COM

PMC-Sierra's MIPS-based processors target metropolitan-transportation, storage-area-networking, wireless-equipment, VOIP (voice-over-Internet Protocol), Internet-routing-equipment, enterprise-switch, and multifunction- and laser-printer applications. The MSP (multiservice-processor) family targets use in CPE (customer-premises equipment), such as wired and wireless VOIP-terminal adapters, home gateways, voice-enabled routers, and NAS (network-attached storage).

★RABBIT SEMICONDUCTOR, WWW.RABBIT.COM

Rabbit Semiconductor, a Digi International company, provides high-performance, 8-bit microprocessors and development tools for embedded control, communications, and Ethernet connectivity. Rabbit offers embedded-design systems, including low-cost development kits, and technical support for both hardware and software.

★RAMTRON, WWW.RAMTRON.COM

Ramtron's FRAM (ferroelectric-random-access-memory)-enhanced Versa 8051 microcontrollers combine a high-performance SOC (system on chip) with nonvolatile FRAM. FRAM writes at bus speed with virtually unlimited endurance and low power for guaranteed data integrity in systems that require rapid and frequent writes and low power consumption. Versa 8051 microcontrollers let designers upgrade 8-bit applications without a costly investment in a new architecture and code.

★RENESAS TECHNOLOGY, WWW.RENESAS.COM

Renesas' processor offerings for embedded-systems extend from low-power, 8- and 16-bit microcontrollers to high-performance, 32-bit microprocessors. New devices in the R8C/Tiny series, the R8C/2X group, target electronic ballasts, handheld power tools, and motor-control systems. Devices in the R8C/3x group target automotive-body-control applications and operate from 1.8 to 5.5V. They feature data-transfer controllers for efficient data movement and background-operation functions for flash rewrites without CPU intervention. New in the H8 series, the H8S/2153 targets advanced communication equipment, and the H8SX/2164 targets baseboard-management-controller applications. In the M16C series, the 50 new microcontrollers in the 64-MHz R32C/100 series incorporate advanced peripherals, such as FlexRay controllers.

New in the SuperH series, the 200-MHz, 400-MIPS SH72544R targets next-generation automotive power trains with 2.5 Mbytes of flash memory, and the SH7262 and SH7264 microcontrollers target digital-audio systems, media-player accessories, and graphical-display applications with 1 Mbyte of SRAM. Three new processors in the SH7730 series for industrial applications include FPUs (floating-point units) and MMUs (memory-management units). The 300-MHz, 540-MIPS SH77650 for in-vehicle-image-recognition-processing applications has a 2.8-GFLOPS FPU that supports single- and double-precision calculations.

Renesas Technology this year added two products to the SH-Mobile series of application processors. The 266-MHz SH-MobileL3V2 handles many video formats and provides a high-resolution-video-capture capability and enhanced functions for controlling image quality. The SH-MobileR2 targets use in personal-navigation devices, portable media players, and video and VOIP (voice-over-Internet Protocol) terminals.

The new BLDC (brushless-direct-current) reference platform handles a variety of algorithms for controlling BLDC motors. The E100 emulator for M16C, H8SX, H8S, H8, and R8C devices allows real-time in-circuit emulation at bus-cycle speeds as high as 130 MHz. The subatomic-particle-board demonstration platforms for the M16C, R8C, and H8 microcontrollers facilitate device familiarization and accelerate system design. Other new support products are available from third-party suppliers.

Renesas' RX architecture includes the RX600 series, which will debut in the second quarter of 2009. These 200-MHz devices support 100-MHz single-cycle flash-access speed. They include a memory-protection unit, and the microcontrollers will be upward-compatible with Renesas' current product lines.

★SAMSUNG ELECTRONICS, WWW.SAMSUNGSEMI.COM

Samsung offers 16- to 32-bit processors targeting handheld-system applications, including smartphones, VOIP (voice-over-Internet Protocol) phones, portable GPS (global-positioning-system) devices, gaming systems, and PDAs (personal digital assistants). Samsung's family of mobile application processors features ARM-920T-, ARM926EJ-, and ARM1176-based RISC cores. Samsung developed the processor family using CMOS-standard cells and a memory compiler.

★SEMTECH, WWW.SEMTECH.COM

Semtech acquired Xemics in 2005 and offers that company's 8- to 22-bit microcontrollers that interface sensors and radio transceivers and target autonomous, battery-operated, wireless devices. These devices operate at a constant one instruction per clock that is independent of the type of operation and addressing mode. The Radio Machine device for ISM (industrial/scientific/medical)-band-transceiver interfacing includes a low-power RISC core with the BitJockey, a serial interface for radio protocols, and a UART. Semtech offers tools and application notes for radio development. The Sensing Machine device for sensor interfacing includes a low-power RISC core with the high-resolution ZoomingADC sigma-delta ADC and a programmable preamplifier.

★SILICON LABORATORIES, WWW.SILABS.COM

Silicon Labs offers a diverse portfolio of mixed-signal, 8-bit microcontrollers. This year, the company introduced its low-voltage, low-power family of devices that can operate at voltages as low as 0.9V. With both a dc/dc controller and a low-dropout regulator on-chip, the C8051F9xx family supports a fast-wake-up-time, low-ac-

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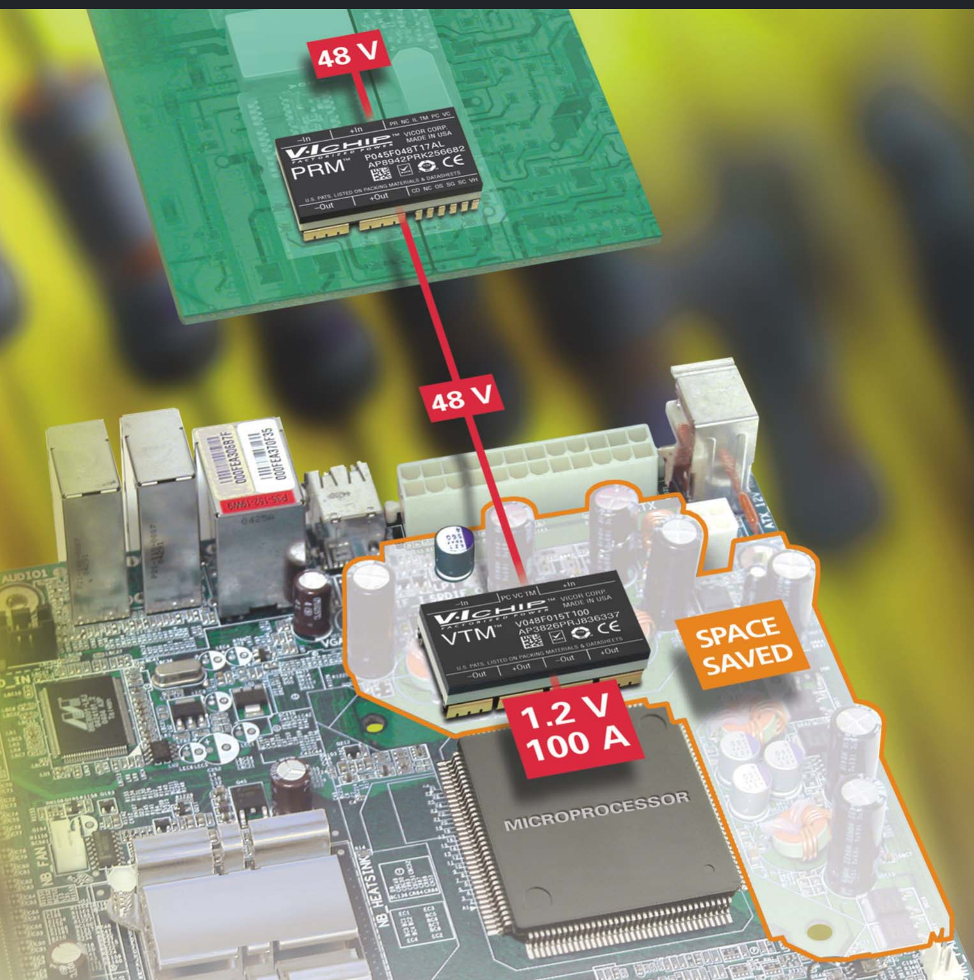

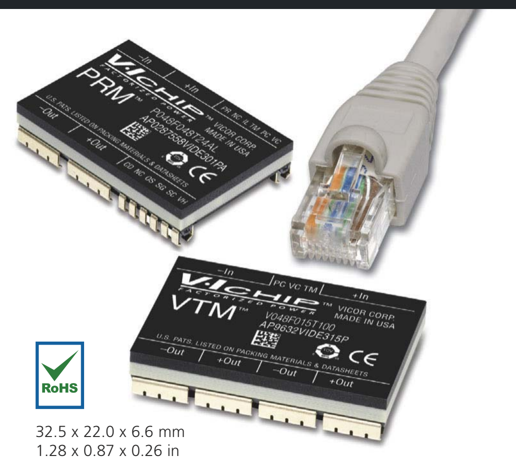

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P045F048T32AL	48	38 – 55	320	97

VTM Model Number	Vout Nominal (V)	Vout Range (V)	Iout (A)	Efficiency @50% Load (%)
V048F015T100	1.5	0.81 – 1.72	100	91.0
V048F020T080	2.0	1.08 – 2.29	80	94.2
V048F040T050	4.0	2.17 – 4.58	50	94.8
V048F120T025	12.0	6.50 – 13.75	25	95.1

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DESIGN NOTES

4-Phase Boost Converter Delivers 384W with no Heat Sink

Design Note 453

Victor Khasiev

Introduction

High power boost converters are becoming increasingly popular among designers in the automotive, industrial and telecom industries. When power levels of 300W or more are required, high efficiency (low power loss) is imperative in the power train components to avoid the need for bulky heat sinks and forced-air cooling. Interleaving power stages (multiphase operation) improves efficiency and reduces ripple voltage and currents in both the input and output capacitors, allowing the use of smaller filter components.

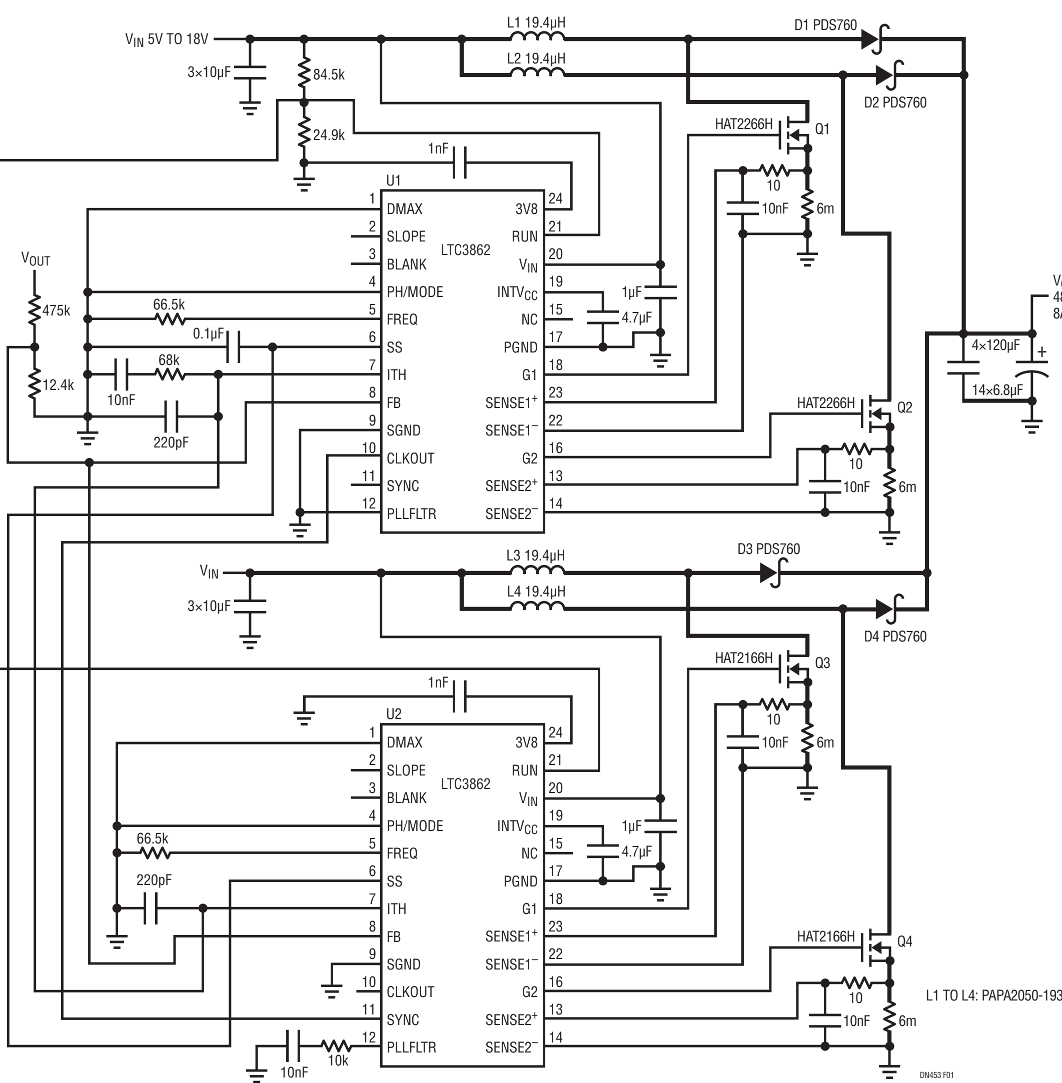

Figure 1. A 4-Phase Boost Converter Based on the LTC3862 Produces 48V at 8A from a 5V to 18V Input

384W Boost Converter

Figure 1 shows a 4-phase boost converter using two 2-phase LTC®3862 current mode controllers configured in a master-slave configuration (as described in the LTC3862 data sheet). U1 is the master controller; it generates the clock signal that serves to synchronize the two controllers. Synchronization is achieved by connecting U1's CLKOUT pin to U2's SYNC pin and terminating the PLLFLTR pin of U2 with a lowpass filter. Each controller operates with a 180° phase shift between its two channels, and there is a 90° phase shift between the two controllers as defined by the state of U1's PHASEMODE pin, to form an interleaved 4-phase system as shown in Figure 2.

The power train includes four inductors L1-L4, four MOSFETs Q1-Q4, four diodes D1-D4, along with the input and output filter capacitors. The ITH, FB, SS and RUN pins of the two controllers are connected together, which forces current share balancing and consistent start up timing between the phases, and forces both controllers to turn on at the same input voltage.

This converter can deliver 8A at 48V continuously from a 12V to 18V input. It can even support the 48V output with input voltages down to 5V, at a reduced output current. Figure 3 shows the converter efficiency above 96% for much of the load range. The transient response to a 3A load step as shown in Figure 4 has only a 100mV deviation from nominal.

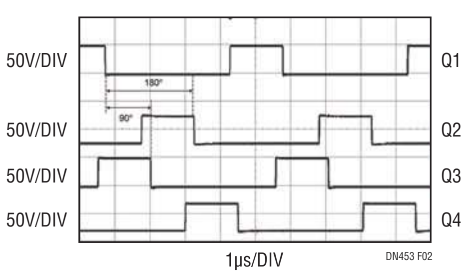

Figure 2. Timing Diagram Showing 4-Phase Operation

Up to 12 power stages can be paralleled and clocked out-of-phase for even higher power applications. The LTC3862 has an input voltage range of 4V to 36V and an output voltage that is dependent upon the choice of external components, making it an excellent choice for 12V automotive high power boost converter applications such as audio amplifiers and fuel injection systems.

Conclusion

The LTC3862 2-phase controller is a powerful building block for multiphase boost converter applications that demand high efficiency, low power loss, reduced ripple voltage and currents, and have a small solution size without the need for forced-air cooling or heat sinks.

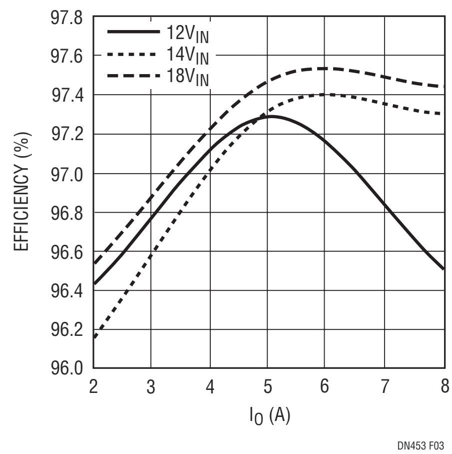

Figure 3. Efficiency vs Output Current Input Voltage for Multiple V_{IN}.

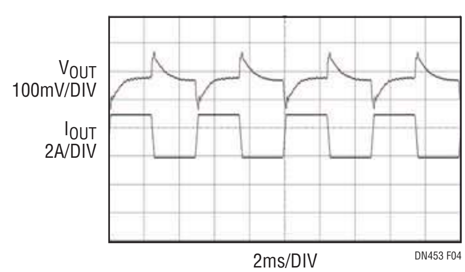

Figure 4. Transient Response for a Current Load Step from 2A to 5A.

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tive-mode, and ultra-low-sleep-mode current consumptions. Silicon Labs has also expanded its family of functionally dense, small-form-factor microcontrollers to include one-time-programmable versions, which are footprint-compatible with the flash-based versions. Silicon Labs developed programming daughtercards as additions to its low-cost ToolStick development platform. Designers can test and debug any Silicon Labs microcontroller using the evaluation platform through a USB (Universal Serial Bus) interface and then plug in the new adapter to program the device.

★SILICON STORAGE TECHNOLOGY, WWW.SST.COM

Silicon Storage based its FlashFlex family of 8-bit microcontroller products on the company's SuperFlash CMOS-semiconductor-process technology. These microcontrollers implement the 8051 instruction set and are pin-for-pin compatible with standard 8051 microcontroller devices. FlashFlex devices are available in single- or dual-block configurations, and they are ISP (in-system-programmable) and IAP (in-application-programmable). These microcontrollers target consumer, communication/wired, imaging and video, audio, industrial, and motor-control applications.

★STMICROELECTRONICS, WWW.ST.COM

STMicroelectronics offers 8-bit microcontrollers and high-performance, 32-bit ARM-based microcontrollers. The company also offers development support through a combination of development tools, training courses, consultancy, and Web support. The 32-bit STM32 family, which is powered by an ARM Cortex-M3 processor, now provides 46 fully compatible devices with 32 to 512 kbytes of flash; 6 to 64 kbytes of SRAM; and new features for displays, sound, storage, and advanced control. The 72-MHz Performance Line stresses new levels of performance and energy efficiency. The 32-bit Access Line stresses 32-bit processing at a 16-bit cost.

The new, advanced, 8-bit STM8 core will be the foundation of a number of new, cost-effective 8-bit-microcontroller families. The first general-purpose family, the STM8S, combines the core's high speed, performance, and code efficiency with peripherals and features for robustness and reliability. Integrated flash options for these devices range from 4 to 128 kbytes.

★STRETCH, WWW.STRETCHINC.COM

Fabless-semiconductor company Stretch provides software-configurable processors for computationally intensive applications. Stretch's S6000 series targets high-speed video and image processing. With these applications in mind, Stretch has developed two reference-design kits using S6000 family software-configurable processors, a PCIe (peripheral-component-interconnect-express) DVR (digital-video recorder), and an IP (Internet Protocol) camera.

★TENSILICA, WWW.TENSILICA.COM

Tensilica offers 32-bit, customizable data-plane processors, DSPs, and standard processor cores. Designers can mold Tensilica's Xtensa processors to fit the application by selecting and configuring predefined elements of the architecture and by inventing new instructions and hardware execution units. Tensilica's processor cores come with software-tool chains that automatically match any changes a designer makes.

This year, the company introduced its smallest controller, the extremely low-power Diamond 106Micro. The company expanded its audio-codec support for the HiFi 2 audio engine with support for MPEG-4 BSAC (bit-sliced arithmetic coding), DTS (digital-theater-sound) audio, Dolby TrueHD (high definition), Dolby digital consumer encode, Dolby digital-compatible output 5.1-channel encode, Spirit DSP, MPEG-4 AAC-LC (Advanced Audio Codec-low complexity), and MPEG-4 AACPlus. Tensilica enhanced the Xenergy energy-estimator tool with a new interface, and the company now supports open-source Linux.

★TERIDIAN SEMICONDUCTOR, WWW.TERIDIAN.COM

Teridian Semiconductor designs, sells, and provides engineering support for its mixed-signal ICs, which find use in energy, automation, networking, and secure-access systems. These ICs connect its customers' digital systems to the analog inputs in utility-metering, industrial-automation, set-top-box, digital-TV, VOIP (voice-over-Internet Protocol), electronic-identity, and point-of-sale applications. Teridian recently announced the availability of its 78Q8430 10/100 Fast Ethernet multimedia-offload controller for general sampling. The device targets video-streaming and mixed-media applications, including data, voice, and video over IP. The 78Q8430 targets Ethernet applications requiring reliable connectivity and QOS (quality-of-service) levels, such as industrial-networking, set-top-box, digital-television, and other consumer-broadband or audio/video equipment. The 71M653x family includes residential-single-phase and commercial- and industrial-three-phase ICs, offering as much as 256 kbytes of storage with 10-MIPS processing power, advanced power management, LCD-contrast adjustment, and a 0.5-sec or 0.5-day hardware real-time clock that consumes only 0.5 μA.

★TEXAS INSTRUMENTS, WWW.TI.COM

Texas Instruments' products range from the ultralow-power, 16-bit MSP430 microcontrollers to the 32-bit, ARM-based microcontrollers and high-performance TMS320C2000 controllers. The company added five new devices to the

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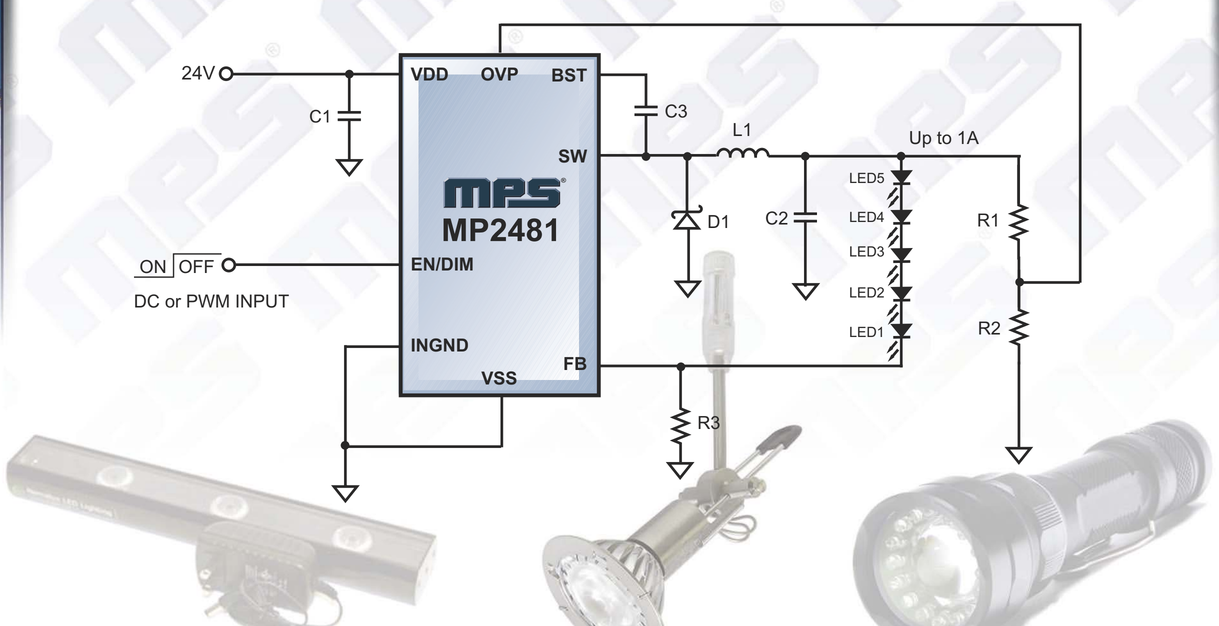

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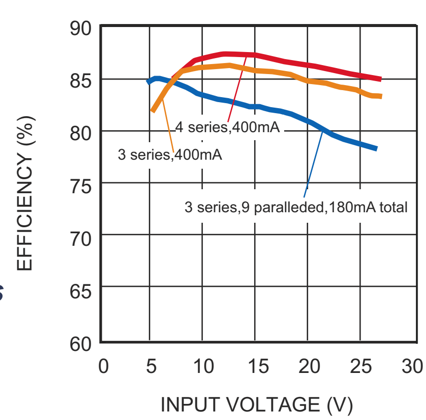
Efficiency vs. Input Voltage

Step-up/down Application



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MSP430F2xx-microcontroller generation, which offers power consumption as low as 500 nA in standby mode. The new devices include general-purpose F2xx devices and microcontrollers for low-power ZigBee networks and devices targeting IEEE 802.15.4-wireless-network and automatic-meter-reading applications.

The new generation of MSP430F5xx microcontrollers offers as much as 25 MHz of performance, additional memory and on-chip peripherals, active power consumption as low as 160 µA/MHz, and standby power consumption as low as 1.5 µA. The F5xx devices enable the ability to use smaller batteries or no batteries for energy-harvesting systems that operate using solar power, vibration energy, or human-body heat.

Building on the previous year's introduction of F2833x floating-point controllers, Texas Instruments announced a hardware- and software-compatible TMS320F282x-controller series. The new series of TMS320F2080xx controllers, code-named Piccolo, offers 32-bit real-time control in a 38-pin package and at a less-than-$2 (high-volume) price. Lower prices and control-optimized accelerators target cost-sensitive applications, such as solar power, LED lighting, white goods, and industrial-motor control.

In 16-bit-development-tool news, the company announced its first wireless-microcontroller-system-development tool, the eZ430-RF2500, which includes all the hardware and software you need to develop a stand-alone-wireless project. Available in a USB (Universal Serial Bus)-stick form factor for $49, the new tool offers two RF-enabled microcontroller-target boards and a PC-debugging interface. The eZ430-RF2500 tool suits sensing, metering, home-security and -automation, and medical applications.

Also supporting 16-bit MSP430 devices, the company released CCEssentials (Code Composer Essentials) Version 3, providing significant upgrades to the previous Eclipse-based CCEssentials IDE (integrated development environment) to enhance performance, emulation, and ease of use at a low cost.

Texas Instruments' five new experimenter and application-specific development kits for its TMS320F28x controllers enable rapid prototyping for communications-infrastructure, industrial, and consumer applications with interchangeable processor-card modules, control cards, or experimenter kits with breadboard areas for full access to device signals in addition to application-specific dc/dc and ac/ac digital-power-developer kits. Each kit includes code examples and full hardware design details, along with the 32-kbyte CCStudio (Code Composer Studio) limited IDE.

★TILERA, WWW.TILERA.COM

Tilera offers high-performance multicore processors targeting embedded networking, security, and multimedia-processing applications. The Tile processor family targets applications requiring packet processing for layers 2 through 7 and for HD (high-definition)-video applications. The Tile64 processor SOC (system on chip) has 64 processor cores plus system-integration blocks. The device includes 5 Mbytes of cache, and each processor core can independently run a full operating system, such as Linux. Tilera based the Tile64 family on a tiled multicore architecture with a mesh-based on-chip interconnect. The mesh architecture delivers as much as 32 Tbps of interconnect bandwidth between the cores and allows scaling the architecture beyond hundreds of cores.

★TOSHIBA AMERICA ELECTRONIC COMPONENTS, WWW.TOSHIBA.COM/TAEC

Toshiba offers highly integrated, 8-, 16-, and 32-bit CISC microcontrollers with embedded SuperFlash memory and 32- and 64-bit, MIPS-based TX RISC microprocessors. TX RISC microcontrollers suit calculation-intensive applications that require large memory capacity and DSP-like functions, such as consumer digital-camera lenses, digital camcorders, and automotive-air-bag systems. Both the CISC and TX families have peripherals for handheld information consoles, home-security systems, calculators, toys, HVAC (heating/ventilation/air conditioning), instrumentation, digital TV, IP (Internet Protocol) set-top boxes, home-entertainment gateways, white goods, and automotive-body controls. A variety of low-cost reference boards, compilers, debuggers, and software drivers that support various operating systems provide support for Toshiba's microcontrollers.

Toshiba's 32-bit TMPA910CRAXBG ARM926-EJS core, features 200-MHz performance and a touchscreen controller, an STN/TFT (supertwisted-nematic/thin-film-transistor) color-LCD controller, an LCD-data-process accelerator, a 10-bit ADC, a NAND-flash controller, an SD (secure-digital) host controller, and a USB (Universal Serial Bus) device controller. Target applications for the TMPA910CRAXBG include networking systems, industrial systems, and consumer electronics, including game consoles, set-top boxes, portable GPS (global-positioning-system) units, and handheld media players.

The 32-bit, 80-MHz TMP92CZ26AXBG CISC-based microcontroller features a built-in LCD controller, a 288-kbyte embedded RAM, a MAC (media-access controller), a 10-bit ADC, and a USB-device controller. It targets applications, such as industrial devices, requiring intensive calculations, high performance, and broad feature support.

Toshiba continues to support its family of 8-bit, low-power microcontrollers with TLCS-870/C1 cores that process one instruction in a single clock cycle, with built-in low-voltage-level detection and power-on-reset capability. The company's first TLCS-870/C1-based product, the general-purpose, 8-bit TMP89FS60UG/FG

EMBEDDED SERIAL NOR FLASH MEMORY

Product	Erasable Sector	Speed	Density
M25P†	256 Kb - 2 Mb	50 MHz, 75 MHz	512 Kb - 128 Mb
M25PX	4 KB, 64 KB	75 MHz (Dual I/O)	8 Mb - 64 Mb
M25/M45PE	256 B, 4 KB, 64 KB	50 MHz, 75 MHz	1 Mb - 16 Mb

EMBEDDED PARALLEL NOR FLASH MEMORY

Product	Voltage	Performance	Density
J3 v.D	2.7V - 3.6V	X8, X16 Page	32 Mb - 256 Mb
P30	1.7V - 2.0V, 1.7V - 3.6V	X16 52 MHz Burst	64 Mb - 512 Mb
P33	2.3V - 3.6V	X16 52 MHz Burst	64 Mb - 512 Mb
M29W†	2.7V - 3.6V	X8, X16 Page	4 Mb - 128 Mb
M58BW†	2.7V - 3.6V, 2.5V - 3.3V (55ns)	X32 Burst	16 Mb - 32 Mb

EMBEDDED NAND FLASH MEMORY

Product	Voltage	Page Size	Density
SLC small page	1.8V/3V	512 B	128 Mb – 1 Gb
SLC large page	1.8V/3V	2 KB	1 Gb - 8 Gb
CompactFlash* card	3V/5V	2 KB	64 MB - 4 GB
eMMC*	1.8V/3V	2 KB	1 GB

*Other names and brands may be claimed as the property of others.
†Automotive temp available.

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microcontroller, combines 60 kbytes of SuperFlash with an eight-channel LED driver, 3 kbytes of RAM, serial-communication interfaces, and a 10-bit ADC in a low-cost QFP.

★TRANSMETA, WWW.TRANSMETA.COM

Although Transmeta no longer manufactures microprocessors, it offers its microprocessor IP (intellectual property) for license. The Crusoe processor targets extreme low power with a balance of performance and cost. Crusoe supports Microsoft and Linux embedded operating systems and other real-time operating systems. Transmeta's second-generation Efficeon processor expands on the performance range that Crusoe offers.

★UBICOM, WWW.UBICOM.COM

Ubicom develops communications and media processors and software platforms that target real-time interactive applications and multimedia-content delivery in the digital home. The company provides to OEMs optimized system-level products, including wireless routers, access points, bridges, VOIP (voice-over-Internet Protocol) gateways, connected digital-photo frames, and streaming-media devices. This year, Ubicom introduced its reference design for wirelessly connected digital-photo frames, which it based on the StreamEngine 5000 family of multithreaded processors. The processors' DSP extension provides accelerated image processing to create sophisticated photo effects. Ubicom also introduced the StreamEngine 7000 series of processors, which delivers nearly twice the performance with lower power in a smaller package than the StreamEngine 5000 family.

★VIA TECHNOLOGIES, WWW.VIA.COM.TW OR WWW.VIATECH.COM

Via offers power-efficient processors targeting x86-based personal electronics and embedded devices with feature-rich digital-media-chip sets. Via divides its processors into five product families that it bases on power-consumption and performance criteria ranging from fanless operation to power-saving capabilities for battery-operated mobile devices. The families are the C7 and C7-M mobile, the fanless Luke, the Eden-N and fanless Eden ESP, the C3-M mobile, and the C3 processors.

★NEW WESTERN DESIGN CENTER, WWW.WESTERNDESIGNCENTER.COM

Western Design Center licenses its 65xx microprocessor IP (intellectual property). The company's product line includes the 8-bit W65C02SRTL and 8/16-bit W65C816SRTL licensable IP. In addition to IP, the company offers 8- and 8/16-bit processor devices. A development-tool suite that includes ANSI/ISO-standard C compilers supports all of the company's products.

★XILINX, WWW.XILINX.COM

Xilinx offers embedded processors, FPGA platforms, and development tools that target aerospace and defense, wired- and wireless-communications, automotive, audio- and video-broadcast, industrial-control, test-and-measurement, and consumer applications. The Virtex family of FPGAs includes the PowerPC 32-bit hard core. The configurable, general-purpose, 32-bit MicroBlaze soft core is available for use with the Spartan family and Virtex-platform FPGAs. Designers can supplement this core with coprocessing capabilities and a tightly integrated FPU (floating-point unit) and by implementing direct connections to hardware instructions in FPGA-logic gates.

★NEW XMOS, WWW.XMOS.COM

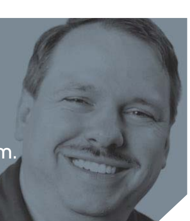
XMOS provides a new type of programmable chip, software-defined silicon, which the company based on an array of high-performance, event-driven processors. You create designs in high-level languages, delivering hardware performance from a software-based design flow. XMOS devices blend a high-performance processor architecture with a responsive I/O structure to provide designers custom silicon that solves a class of design problems.

This year, the company shipped the four-core XS1-G4 device and opened access to its Web-based design tools. The G4 device supports 32 concurrent real-time tasks and services 400 million events/sec. In July, the company shipped the XS1-G development kit, which supports a complete hardware/software environment with no need to build test boards or evaluation hardware. Most recently, XMOS launched the Xlinkers design forum (xlinkers.org) for developers interested in XMOS technology and in sharing their knowledge, ideas, and code examples.

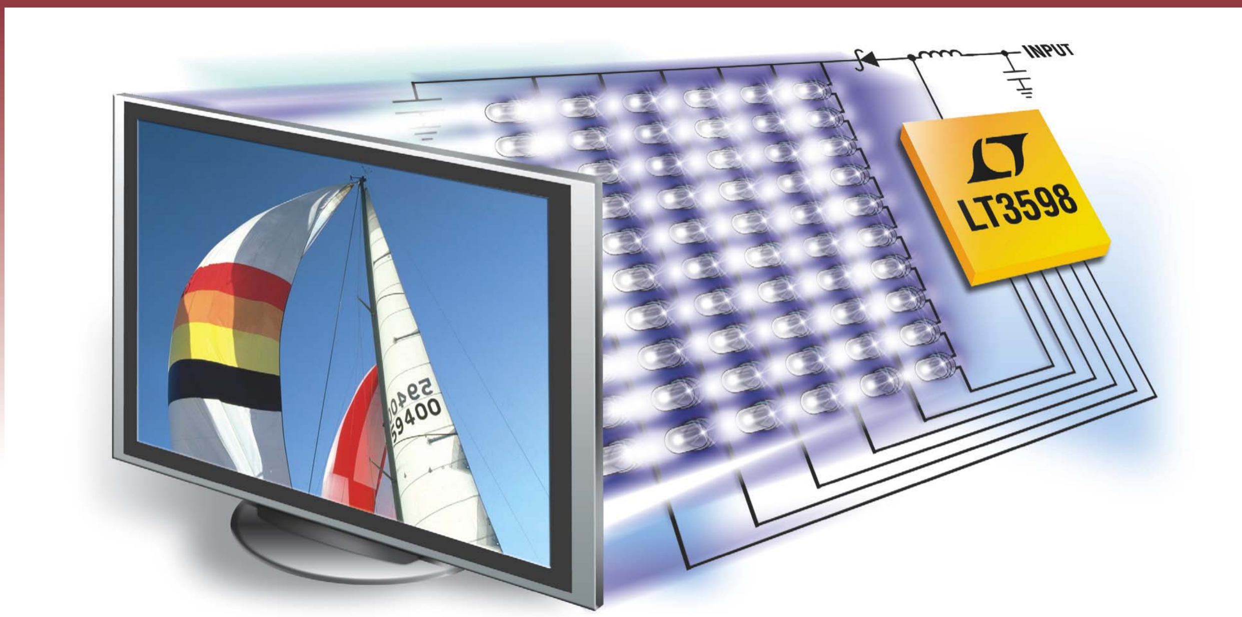
★ZILOG, WWW.ZILOG.COM

Zilog offers 8-, 16-, and 32-bit microprocessors. The company's Zbase remote-control code database, Crimzon products, and engineering services support designers of universal-remote-control devices. The ARM-based Zatara family of products targets the banking industry's requirement for all POS (point-of-sale) systems to comply with PCI (payment-card-industry) PED (PIN-entry-device) standards. Zatara devices also target adjacent markets, such as PIN (personal-identification-number) pads, ATMs (automatic teller machines), gas pumps, kiosks, and other POS terminals.

You can reach Technical Editor Robert Cravotta at 1-661-296-5096 and rcravotta@edn.com.



Light Up 60 LEDs



$36V_{IN}$, 2.5MHz, 3000:1 PWM Dimming Range LED Driver

Many small to medium-size panel displays need large numbers of white LEDs for backlighting. Powering and driving up to 16W for these LEDs is challenging due to size and thermal constraints. With the LT®3598 and LT3599, the solution just got easier. These multiple-string LED drivers deliver up to 16W (7W for LT3598) of power and allow a 3000:1 dimming range for brightness adjustment, high LED current accuracy for uniformity of light output, good thermal and LED protection features for a rugged, compact design.

Features

- LT3598: Drives 6 Strings of LEDs at up to 30mA per String
- LT3599: Drives 4 Strings of LEDs at up to 100mA per String
- 1% Accurate LED Current Regulation
- Wide V_{IN} Range: 3V to 30V (36V Transient)
- Adjustable Frequency and Synchronization: 200kHz to 2.5MHz
- Regulated LED Current Even When $V_{IN} > V_{OUT}$
- Programmable LED Temp Derating

LT3598 Demo Circuit

Actual Size

Info & Free Samples

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Free Power Management for LEDs Brochure

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LINEAR TECHNOLOGY

DC-accurate, 32-bit DAC achieves 32-bit resolution

W Stephen Woodward, Chapel Hill, NC

Some applications, such as ADC testing and calibration, require a DAC with extremely good resolution, monotonicity, accuracy, and resolution. In these categories of performance, the circuit in **Figure 1** is hard to beat. Its typical specifications follow:

- Resolution=32 bits=3×10^{-10}=1.2 nV=192 dB.
- DNL (differential nonlinearity)=27 bits=400 nV=162 dB.
- INL (integral nonlinearity)=22 bits=1.6 μV=130 dB.
- Full-scale accuracy (untrimmed)=11 bits=±2.5 mV=66 dB.
- Zero accuracy=23 bits=±500 nV±10 nV/°C=140 dB.
- Ripple and noise=21 bits=2 μV p-p=128 dB.

The basis of the DAC's 32-bit resolution is the summing of two 16-bit PWM signals by analog switches S_1 and S_2 and precision resistor network R_2 through R_6. The DAC's monotonicity and DNL are theoretically infinite, and, in practice, the only limit is the 1-to-2^{16} ratio of R_2: $(R_6+R_5+R_{S2\text{-}ON})$ and R_3: $(R_6+R_4+R_{S2\text{-}ON})$. Typical accuracy of 0.1% resistors yields a DNL of approximately 0.1 ppm=27 bits.

The less-than-0.1Ω output impedance of the AD586 reference and the 130-dB CMR (common-mode rejection) of chopper-stabilized "zero-drift" amplifier A_1 mostly limit INL. R_7 suppresses a potential contribution from asymmetry in $R_{S1\text{-}ON}$, yielding the typical INL of approximately 0.3 ppm=22 bits.

DIs Inside

62 Digitally programmable instrumentation amplifier offers autozeroing

64 C# application controls simple ADC

66 Perform bitwise operation in Excel spreadsheets

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Zero-accuracy and output-noise specs are at the low-microvolt level because of the excellent specifications

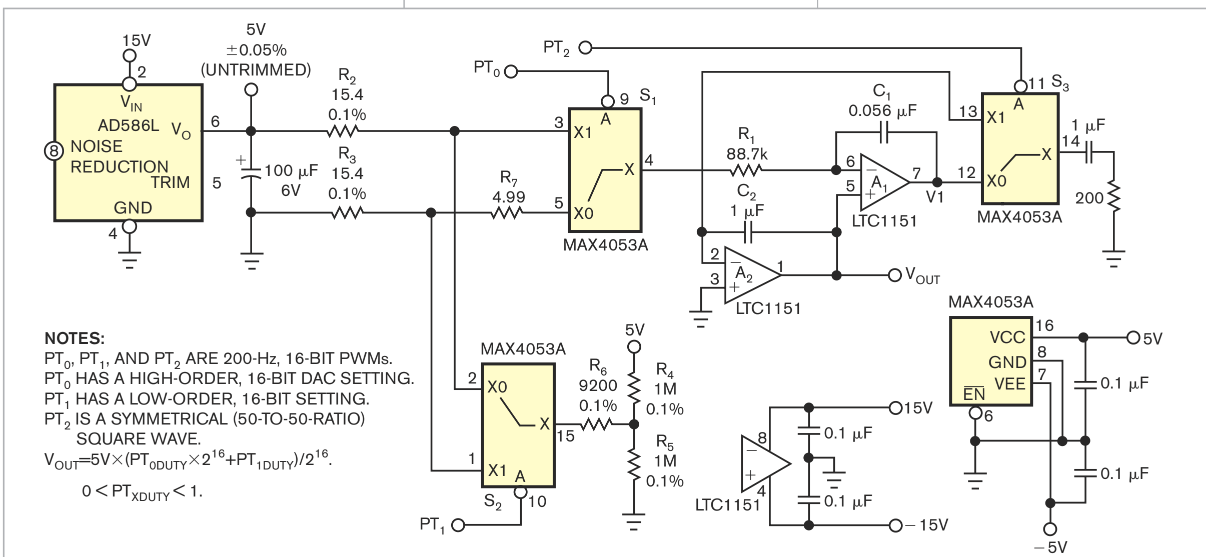


Figure 1 This DAC circuit sums two 16-bit PWM signals using precision analog switches to achieve 32-bit resolution.

of the LTC1151 A_1 and A_2 op amps and the charge-injection performance of the MAX4053A S_2: approximately 0.4 ppm, or 23 bits.

The precision of the AD586L 5V reference, which is ±500 ppm untrimmed, limits absolute accuracy. If your design requires greater accuracy, then you can use an Analog Devices (www.analog.com) simple trim circuit to further tweak it. There's nothing critical about the suggested 200-Hz PWM cycle. You need to change only R_1 and C_1 to accommodate any convenient frequency. How closely the R_1C_1 time constant matches the PWM-cycle time determines the settling time of the A_1-S_2-A_2 synchronous "zero-ripple" integrate-and-hold filter, and can be as fast as one cycle if the match is exact. **EDN**

Digitally programmable instrumentation amplifier offers autozeroing

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

The current trend in advanced instrumentation amps is to use no external resistors. In these amplifiers, a gain-control word, comprising a binary-coded one, sets the voltage gain. Several integer gains within one to 1000 are currently available; however, this range does not yet include a gain of three. Although external-resistor-free amplifiers with a gain of three are available, they are neither instrumentation amps nor autozeroed devices (**Reference 1**). These features are essential in applications requiring accurate processing of low-level voltages. You can use the circuit in **Figure 1** for applications requiring instrumentation amps having voltage gains of three or 10 and the ability to process voltages as low as 1 mV.

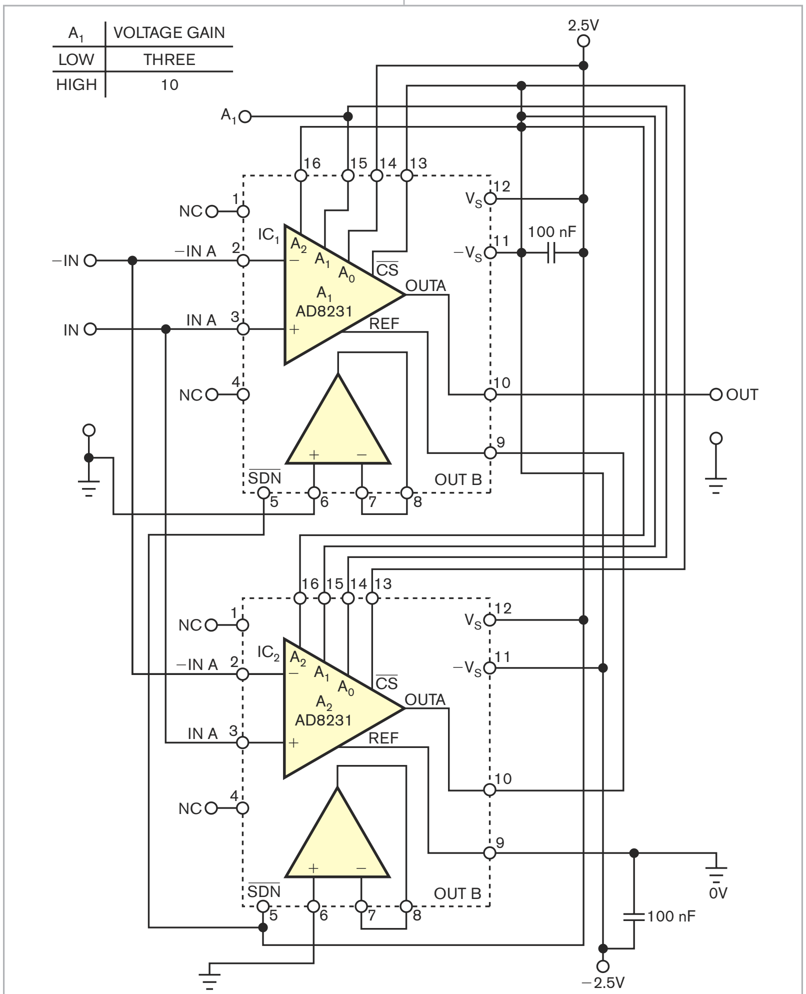
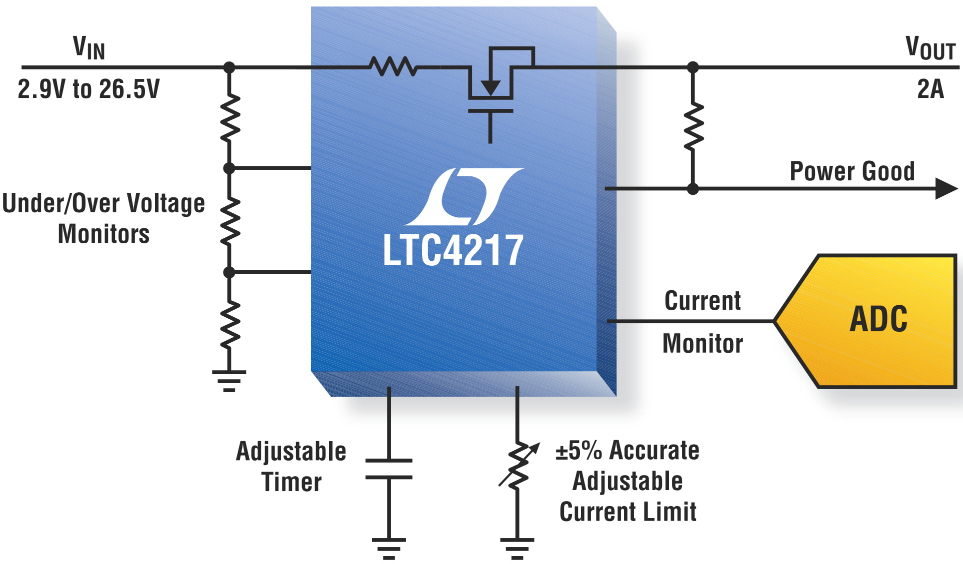


Figure 1 The autozeroed instrumentation amp, digitally programmable for voltage gains of three and 10, can help you to overcome the current inavailability of monolithic ICs for this task.

This design achieves a voltage gain of three by using the "algorithm" of 3=2+1. The circuit comprises two units of the Analog Devices (www.analog.com) digitally gain-programmable, autozeroed AD8231 instrumentation amp. These ICs have voltage gains that are programmable as powers of two—that is, one, two, four ... 128 (**Reference 2**). Amplifier A_1 in IC_1 is preset to provide a gain of two, and auxiliary amp A_2 in IC_2 is preset to a gain of one. The noninverting and inverting inputs of A_1 and A_2 connect together. The output of A_2 connects with reference input REF_1, and reference input REF_2 serves as a freely usable reference. You can thus calculate the output voltage as $V_{OUT}=V_{OUT1}+V_{REF1}=V_{OUT1}+V_{OUT2}=2\Delta V_{IN}+\Delta V_{IN}=3\Delta V_{IN}$, where ΔV_{IN} is the input-difference voltage.

Similarly, you can achieve a voltage gain of 10 according to a symbolic formula of 10=8+2. This time, A_1 has a voltage gain of eight, and A_2 has a gain of two. Using **Reference 2**, you can derive that, for gains of both three and 10, $A_{1A1}=A_{0A2}$. Therefore, the gain-control pins connect and remain low for a gain of three, and the high at

Hot Swap Controller–Fully Loaded



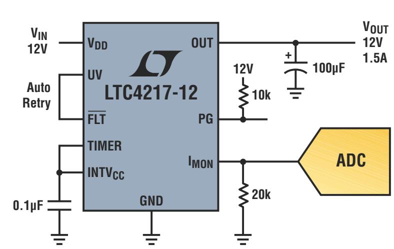
Compact Solution Integrates 2A FET & R_{SENSE}

Our low voltage Hot Swap™ Controllers limit inrush current, provide overcurrent protection during normal operation and provide a slew of supervisory features. Their high accuracy current limit minimizes supply overdesign in RAID, ATCA and AMC systems. The LTC®4217's integrated 2A MOSFET and 7.5mΩ sense resistor, along with UV, OV, Powergood and Current/Temperature/Fault outputs, reduce component count in space-constrained designs and maintain healthy card operation in harsh environments.

Features

- Small Footprint
- 25mΩ MOSFET and 7.5mΩ R_{SENSE}
- Wide Operating Voltage Range: 2.9V to 26.5V
- Adjustable, 5% Accurate (2A) Current Limit
- Current and Temperature Monitor Outputs
- Overtemperature Protection
- Adjustable Current Limit Timer Before Fault
- Powergood and Fault Outputs
- 20-Lead TSSOP and 16-Pin 5mm x 3mm DFN Packages

LTC4217-12 Dedicated 12V Version



- *Preset 12V Thresholds*
- *Accurate OV, UV and Current Limit Thresholds*
- *Fewer External Components*
- *Minimizes Cost and Complexity*

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these pins sets the gain to 10. Note that three approaches the square root of 10, or approximately 3.16. You can therefore consider it as roughly the geometric center of a decade.EDN

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2 "Zero Drift, Digitally Programmable Instrumentation Amplifier, AD8231," Analog Devices Inc, 2007, www.analog.com/en/prod/0,2877,AD8231,00.html.

C# application controls simple ADC

Yury Magda, Cherkassy, Ukraine

This Design Idea describes a simple and low-cost ADC that you control using the serial port of a PC running Windows XP/Vista. The hardware comprises Microchip's (www.microchip.com) 12-bit SAR (successive-approximation-register) MCP3201 ADC, which attaches to the serial port of the PC through the RTS, CTS, and DTR lines (**Figure 1**).

The circuit uses an SPI (serial-peripheral-interface)-compatible interface to communicate with the MCP3201. The MAX232 chip transforms the RS-232 levels into TTL-compatible levels that the MCP3201 converter requires to operate. The analog signal comes through the IN+ pin of the MCP3201. The output digital stream of bytes on the D_{OUT} pin goes through the CTS line to the serial port of the PC. The RTS line of the serial port provides clock pulses that go through the CLK pin of the converter. Each separate bit appears on D_{OUT} on the falling edge of CLK, and the application should latch the bit on the rising edge of the clock pulse.

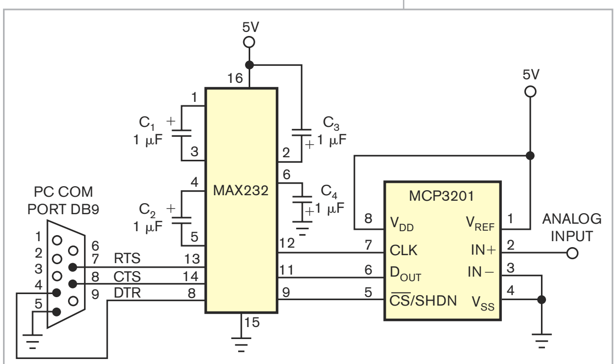


Figure 1 This simple, low-cost ADC comprises a 12-bit SAR ADC, which attaches to the serial port of the PC through the RTS, CTS, and DTR lines.

The DTR line produces the $\overline{CS}$ signal that frames the conversion process. The $\overline{CS}$ signal must be low while the conversion is in progress (**Figure 2**).

The meaningful bits, with MSB first, appear on D_{OUT} after the third CLK pulse goes low. It implies that, if you miss the first three data bits, the software would programmatically realize it. The software that controls the device is written in free Microsoft (www.microsoft.com) Visual C# 2008 Express Edition. It uses a built-in SerialPort component that allows you to get full control over the serial port of the PC. You implement the software as a simple console application containing **Listing 1**, which is available with the Web version of this Design Idea at www.edn.com/081030di1. The program is uncomplicated, so you can easily modify it. For instance, you could send the data from ADC over the Internet or pass it into Microsoft Excel or Microsoft Access for further processing.

You can improve the simplified circuit in **Figure 1** for higher accuracy by placing a lowpass filter in the analog-signal chain. You should also always use a bypass capacitor with the MCP3201. Place a capacitor with a recommended value of 1 µF as close as possible to the device's pin. You can also replace the MCP3201with a similar SAR ADC that works with an SPI-compatible interface. For instance, you may use an LTC1286 or an LTC1297 device from Linear Technology (www.linear.com). If you plan to use a different ADC, you must

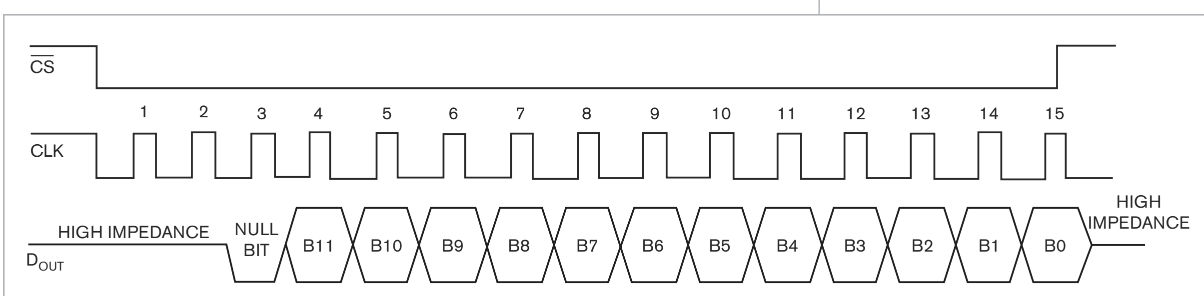
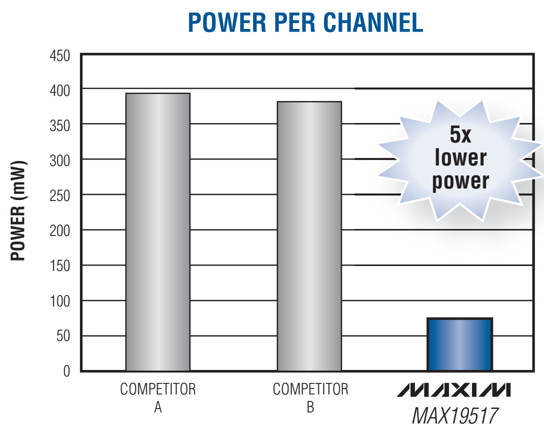


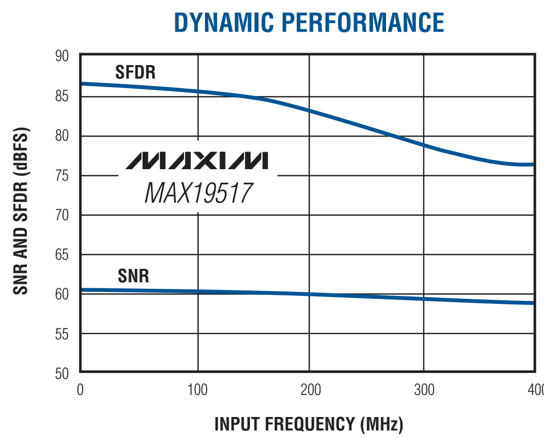
Figure 2 The DTR line produces the $\overline{CS}$ signal that frames the conversion process. The $\overline{CS}$ signal must be low while the conversion is in progress.

Industry's lowest power, dual-channel, 10-bit, 130Msps ADC has superior dynamic performance

Extensive feature set minimizes external component count

The MAX19517 ADC is a member of Maxim's pin compatible family of ultra-low power, dual-channel ADCs. Its extensive set of features (a partial list is shown below) minimizes external component count and supports a wide range of applications that demand high performance.





Selected key features

- Lowest power: 75mW per channel
- Excellent performance for input frequencies from DC to > 400MHz
- Self-sensing supply regulation
- 1.8V, 2.5V, 3.3V operation
- Wide input common-mode range
- Programmable CMOS termination
- Flexible data formatting
- Programmable data timing
- Programmable clock divider: 1x, 2x, 4x
- Data output test patterns
- 7mm x 7mm, 48-pin TQFN package

Pin-compatible, ultra-low-power, dual-channel ADCs

Part	Resolution (Bits)	Sample Rate (Msps)	Power per Channel (mW)	SNR (dBFS)	SFDR (dBFS)
MAX19517	10	130	75	60.0	85
MAX19516	10	100	57	60.0	85
MAX19515	10	65	43	60.0	85
MAX19507*	8	130	75	49.7	69
MAX19506*	8	100	57	49.7	69
MAX19505*	8	65	43	49.7	69

*Future product—contact factory for availability.

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make some changes in the hardware and software. The changes necessary to the hardware are obvious, and you may need to change the software source code of the application to correct the *for* (...) loop statement according to the timing diagram of the selected part.EDN

Perform bitwise operation in Excel spreadsheets

Bruno Muswieck, Eletroeste, Uruguaiana, Brazil

Microsoft's (www.microsoft.com) Excel helps engineers with calculus and graphics to solve problems. But engineers often have to perform bitwise operations, too. **Figure 1** shows the bitwise operations' tables. The bitwise functions work for decimal values. If you need to use hexadecimal or binary values, you must use the Dec2Bin and Dec2Hex functions to convert all the decimal values for the desired format.

To install the add-in bitwise functions, you can download the ins.xla file from the Web version of this Design Idea at www.edn.com/081030di2. In Excel, go to Tools, then Add-Ins, and then Browser. Find the downloaded add-in xla file and click OK. Now, Excel can run the bitwise functions.

You can also download some examples from the *EDN* Web site at www.edn.com/081030di2 (**Reference 1**).EDN

REFERENCE

1 Kagan, Aubrey, *Excel by Example: A Microsoft Excel Cookbook for Electronics Engineers*, Newnes Elsevier, 2004, ISBN 0-7506-7756-2.

AND		RESULT
0	0	0
1	0	0
0	1	0
1	1	1

OR		RESULT
0	0	0
1	0	1
0	1	1
1	1	1

XOR		RESULT
0	0	0
1	0	1
0	1	1
1	1	0

NOT	RESULT
0	255
1	254

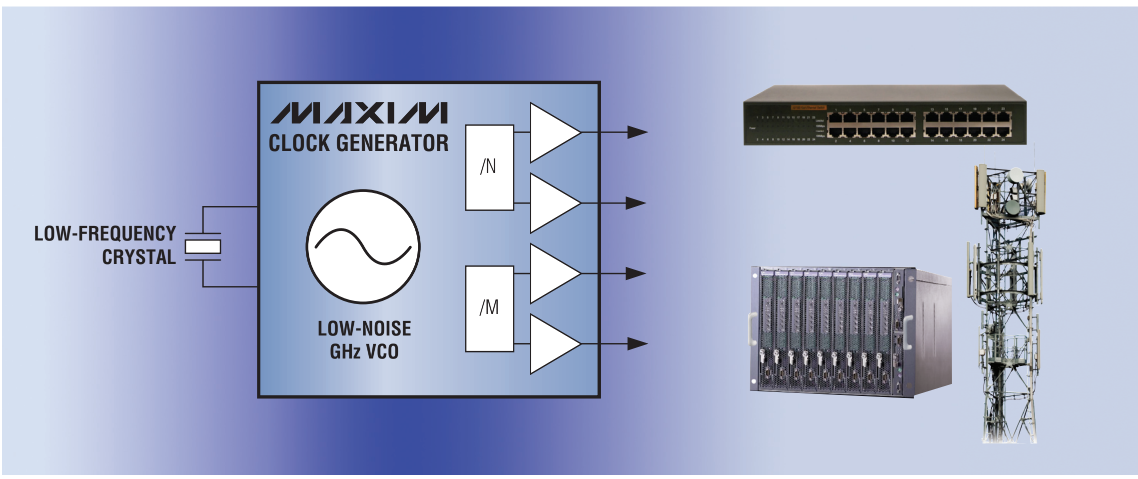
SHIFT RIGHT		RESULT
BINARY	SHIFTED	BINARY
11010010	6	00000011

SHIFT LEFT		RESULT
BINARY	SHIFTED	BINARY
01100100	2	10010000

Figure 1 With the help of some new add-in functions, you can perform these bitwise operations in Excel.

Precision clock solutions speed time to market

Low-jitter, high-frequency clock generators provide frequency flexibility



- **GHz VCO achieves $0.36ps_{RMS}$ (12kHz ~ 20MHz) jitter at high frequencies from inexpensive crystal resonator**
- **-57dBc PSNR minimizes jitter degradation, easing system timing design for noisy environments**
- **Glitchless switching and frequency margining improve system reliability**

Find your low-jitter clock generator at: www.maxim-ic.com/clock-info

<table>
<tr><th rowspan="2">Part</th><th rowspan="2">Feature</th><th rowspan="2">Outputs</th><th colspan="6">Application</th></tr>
<tr><th>Ethernet</th><th>Fibre Channel</th><th>Storage</th><th>Server</th><th>SONET/SDH</th><th>Wireless BTS</th></tr>
<tr><td>MAX3624</td><td>$0.36ps_{RMS}$</td><td>3 LVPECL, 1 LVCMOS</td><td rowspan="3">✓</td><td rowspan="3">✓</td><td rowspan="4">✓</td><td rowspan="4">✓</td><td>✓</td><td>✓</td></tr>
<tr><td>MAX3625</td><td>$0.36ps_{RMS}$</td><td>3 LVPECL</td><td></td><td></td></tr>
<tr><td>MAX3674</td><td>Frequency margining</td><td>2 LVPECL</td><td>✓</td><td>✓</td></tr>
<tr><td>MAX3678</td><td>Glitchless switching</td><td>9 LVPECL</td><td></td><td></td><td></td><td></td></tr>
</table>

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OPTOELECTRONICS/DISPLAYS

Surface-mount LEDs replace through-hole devices

Combining surface-mount technology with the capabilities of through-hole, leaded T-5-mm epoxy-lens LEDs, the OctoLED features 7000-mcd brightness levels. Replacing the 5-mm standard through-hole LEDs, the devices measure 6×6×11 mm and come on 24-mm tape for automatic insertion. Available in a range of colors, including red, yellow, green, blue, and white, the LEDs also come in bicolor and RGB versions. The devices also include a variety of lens finishes, allowing different viewing-angle options, varying depending on lens type. The ROHS (restriction-of-hazardous-substances)-compliant LEDs can withstand 225°C soldering temperatures for 10 seconds, with a recommended 2°/sec gradual temperature rise until reaching 150°C. Prices for the OctoLEDs start at 30 cents, based on color specification.

Lumex, www.lumex.com

Light-management IC integrates LED driver

Aiming at compact-smartphone and portable-media-player applications, the NCP5890 lighting-management device integrates LCD backlighting, light controls, and ambient-light sensing. Providing a 30V output capability, the device drives LEDs to achieve homogeneous backlighting over an LCD screen. The device also controls three sets of white LEDs or RGB LEDs, creating light patterns on keypads or chassis in a unique combination with backlighting. The driver extends battery life by adjusting the backlight current according to the ambient-light level. Available in a 3×3×0.55-mm µQFN-16 package, the NCP5890 costs $1.30.

On Semiconductor, www.onsemi.com

United States Postal Service

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Simon Young, Group Audience Marketing Director, September 22, 2008

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1. Publication Title: EDN

	12-Month Average	September
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Digital Circulation	19,671	19,037
Total Circulation	128,844	127,407

Simon Young, Group Audience Marketing Director, September 22, 2008

EDN ADVERTISER INDEX

Company	Page
Actel Corp	6
Advance Devices Inc	69
Agilent Technologies	11
Analog Devices Inc	21
	23
	C-3
Ansoft Corp	14
Atmel Corp	2
austriamicrosystems AG	66
Bourns Inc	3
Coilcraft	C-4
Cole Parmer Instrument Co	69
Digi-Key Corp	1
EMA Design Automation	43
Express PCB	34
International Rectifier Corp	9
Intersil	47, 49
	50, 51
Keil Software	37
LeCroy Corp	C-2
Linear Technology Corp	60
	63
	53, 54
LPKF Laser & Electronics	36
MathWorks Inc	29
Maxim Integrated Products	65
	67
Mentor Graphics	55
	57
	59
Micrel Semiconductor	12
Microchip Technology	27
Mill Max Manufacturing Corp	45
Monolithic Power Systems	56
Mouser Electronics	8
NAC	34
National Instruments	4
National Semiconductor	46
NewarkInOne	25
Numonyx	58
On Semiconductor	33
Pico Electronics	13
	37
Samtec USA	35
Tern	69
Texas Instruments	17
	19
	40-A-B
That Corp	68
Toshiba America	30
Vicor Corp	52
Xilinx Inc	48

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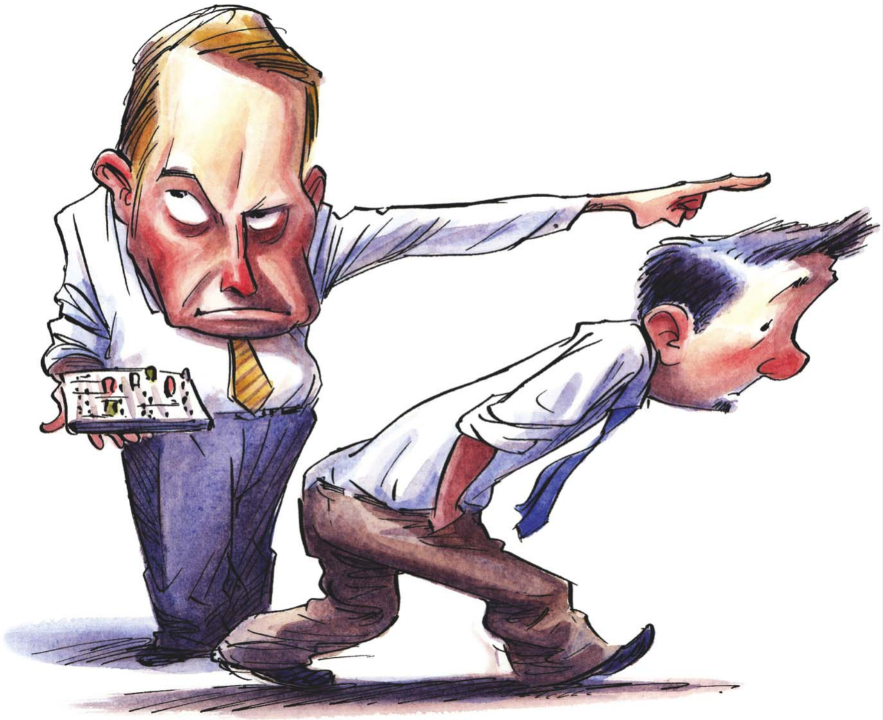
Stick to the schematic



DANIEL VASCONCELLOS

I recently needed to re-create a settling-time-measurement jig I built 25 years ago. It transmits and receives 10V swings and is flat enough and magnifies enough to see 0.01%/division within 35 nsec on an oscilloscope. You can't buy such a step generator, and you can't use an oscilloscope unassisted to see 0.01% absolute-settling features.

I instructed our intern to build it. I made sure that he stuffed only the first stage, which is a wideband differential amplifier employing a 35-year-old CA3127 transistor array from RCA Semiconductor, which General Electric Semiconductor and then Harris Semiconductor absorbed. Now, Intersil has absorbed it, so we have the part in inventory.

He proudly showed it working in the lab. Square waves at the input came out square. He commented, though, that the differential outputs seemed to have a large offset. I checked the operating currents, and they were correct. I then applied a triangle wave to the input. Holy schmaltz! The output was curved! The other of the differential outputs was simply railed—not good. I inadvertently rubbed the board with a finger and saw the entire waveform warp back to triangle shape and shift its dc level.

OK, we had an oscillation there, one that was too fast for our 400-MHz oscilloscope to see. I discovered that I could get any manner of triangle distortion or offset depending on where I touched. A finger presents an impedance of approximately 100 pF in series with approximately 100Ω to ground, and this condition loads and modifies oscillations. A couple of things happen during oscillation. The oscillation grows in amplitude until it overloads devices, causing dc rectification and operating-point shifts. Thus, the offset varies with where you touch your finger. A consequence of this variation is that low-frequency signals variably encounter the dc shift, so gain and offset variations and even nonlinearities on the signal can occur.

The other result of oscillation is radiation, meaning that you can find the oscillation using an antenna and a very-high-frequency-sensitive lab instrument, such as a spectrum analyzer. So, I made a small antenna from a coaxial cable cut and a small loop connecting from the center conductor to the shield. This small transformer secondary coupled energy efficiently enough for a spectrum analyzer to show.

So, holding my loop near the part, I saw a 1.6-GHz spectral spike that disappeared when I powered the system off. I then found that I could put my finger anywhere, even in ground regions, and influence the spectrum. Unfortunately, I couldn't find a place that killed the oscillation. I used a metal probe, fingering down to keep the probe length and inductance low.

The grounds were hot everywhere! I had our intern drill holes in a grid every ¾ in. between top foil and bottom grounds, shorting them all over.

After three sessions, I made no progress, so I looked at the data sheet of the CA3127. The peak gain-bandwidth product was 1.2 GHz. How do you get a 1.6-GHz oscillation from a 1.2-GHz part?

At this point, I didn't trust the part. I asked what part it was, and the intern assured me that it was a 3127—the HFA3127! Looking at that part's data sheet, I noticed an improved 8-GHz array at the gain-bandwidth-product curve, and, although an 8-GHz part can oscillate at 1.6 GHz, our board layout couldn't handle such fast transistors.

He replaced the array with a CA3127, and all was fine—no offset, no distortions. I didn't recommend the HFA devices, so I blamed the intern. EDN

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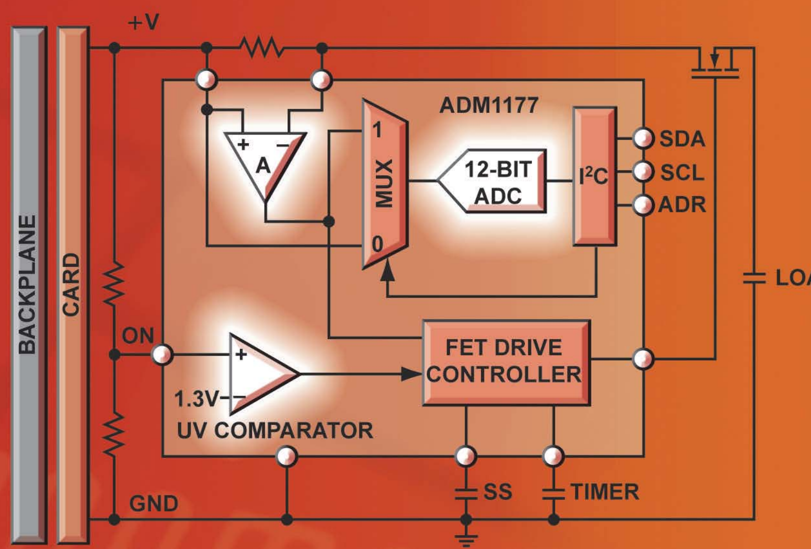

Hot Swap controllers with integrated power monitors

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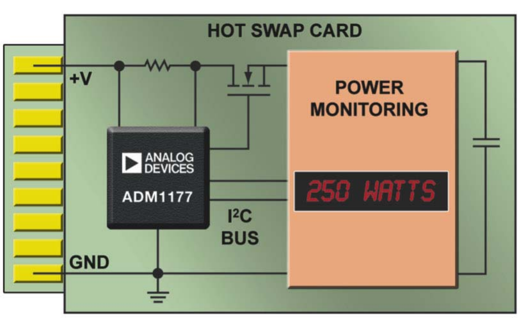
Hot Swap ICs with precision ADC deliver greater accuracy for improved energy savings.



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Let us show you how we're applying more than four decades of analog expertise to power management and delivering industry-best solutions that differentiate your designs and add value for your customers. Case in point: we've integrated industry-leading converter and amplifier cores with Hot Swap controllers to provide unmatched ±3% power monitoring accuracy, allowing you to offer your customers increased energy savings opportunities for data center applications.

Put our analog leadership to work with your power designs. Contact ADI's power technical support at *power.management@analog.com*.

Part Number	Hot Swap Range (V)	Integrated Power Monitoring	Features	Package	Price @ 1k ($U.S.)
ADM1175	3.15 to 16.5	Yes	Manual convert pin	10-lead MSOP	2.50
ADM1176	3.15 to 16.5	Yes	16 I²C addresses	10-lead MSOP	2.50
ADM1177	3.15 to 16.5	Yes	Dedicated SOFT START pin	10-lead MSOP	2.50
ADM1178	3.15 to 16.5	Yes	Overcurrent ALERT pin	10-lead MSOP	2.70
ADM1170	1.6 to 16.5	No	Separate VCC pin	8-lead TSOT	2.10
ADM1171	2.7 to 16.5	No	Current sense output	8-lead TSOT	2.20
ADM1172	2.7 to 16.5	No	Power fail comparator	8-lead TSOT	2.00

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